Keysight U4164A Logic Analyzer

Service Guide

KEYSIGHT TECHNOLOGIES

Notices

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CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Additional Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Safety Symbol	Description
	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australia EMC Framework regulations under the terms of the Radio Communication Act of 1992.
	CE compliance marking to the EU Safety and EMC Directives. ISM GRP-1A classification according to the international EMC standard. ICES/NMB-001 compliance marking to the Canadian EMC standard.
	Product With Toxic Substance 40 yr EPUP
	The crossed out wheeled bin symbol indicates that separate collection for waste electric and electronic equipment (WEEE) is required, as obligated by DIRECTIVE 2012/19/EU and other National legislation. Please refer to about.keysight.com/en/companyinfo/environment/takeback.shtml to understand your Trade in options with Keysight in addition to product takeback instructions.
	This mark denotes compliance with the essential requirements of the following applicable UK regulations: • Electromagnetic Compatibility Regulations 2016 No. 1091 (as amended) • Electrical Equipment (Safety) Regulations 2016 No. 1101 (as amended) • The Restriction of the Use of Certain Hazardous Substances in Electrical & Electronic Equipment Regulations 2012 No. 3032 (as amended)

Keysight U4164A Logic Analyzer - At a Glance

The Keysight U4164A logic analyzer is a 136 channel AXIe based high speed state and timing logic analyzer with new features such as:

- DDR4 and LPDDR4 probing for data rates over 2.5 Gb/s using the new Quad sampling state mode and single touch probing
- Deeper memory
- Quarter channel 10GHz Timing mode
- Deskew of timing traces by individual channels

The module can be used as a general purpose logic analysis system as well as for debug, validation and analysis of DDR and LPDDR memory systems. It allows maximum DQ visibility with simultaneous Read and Write traffic capture for DDR4 and LPDDR4. It supports up to 4 Gb/s State Mode and 10 GHz Timing Mode.

The U4164A has 2 M to 400 M sample memory depth (depending on the license option chosen).

Features

Some of the main features of the U4164A module are as follows:

- 136 channels per module
- Expandable to 408 channels (as a 3-card set in the AXIe chassis).
- A new state sampling clock mode - Quad Sample that allows four samples per clock edge.
- A new Timing (Asynchronous) sampling option - Quarter Channel Timing Mode with the 01G or 02G license.
- 4 Gb/s (2.5 GHz) maximum state acquisition speed (with the "02G" license).
- 2.5 GHz timing analysis in Full Channel timing mode, 5.0 GHz timing analysis in the Half Channel timing mode, and 10.0 GHz timing analysis in the Quarter Channel timing mode.
- A state sampling clock with the following clock qualifiers:
  - Four clock qualifiers - Pods 2, 3, 4, and 5 of the clocking module
  - An additional “RESET” clock qualifier - Pod 7 of the clocking module
- A new setting called Clock hysteresis for the state sampling clock on Pod1 of the U4164A module. Using this setting, you can set a value (in milliVolts) between 0 and 1 volts around the clock threshold.

To know about these features in detail, refer to the U4164A Data Sheet (5992-1057EN) on www.keysight.com and the *Logic and Protocol Analyzer online help* installed with the Logic and Protocol Analyzer software.

Service Strategy

The service strategy for this module is the replacement of defective module/parts. This service guide contains information for finding a defective assembly by testing and servicing the U4164A logic analyzer module.

The modules can be returned to Keysight Technologies for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

Contacting Keysight Technologies

To locate a sales or service office near you, go to www.keysight.com/find/contactus.

Application

This service guide applies to U4164A logic analyzer modules installed in a M9502A or M9505A AXIe chassis.

Figure 1 U4164A Logic Analyzer Module

The following figure displays the M9502A 2-slot AXIe chassis and M9505A 5-slot AXIe chassis.

Figure 2 M9502A and M9505A AXIe Chassis

In This Service Guide

This book is the service guide for the U4164A logic analyzer module.

This service guide has six chapters.

Chapter 1, “General Information” contains information about the module, lists accessories for the module, gives specifications and characteristics of the module, and provides a list of the equipment required for servicing the module.

Chapter 2, “Preparing for Troubleshooting or Performance Testing” tells how to prepare the module for use.

Chapter 3, “Testing U4164A Performance” tells how to verify the U4164A performance with specifications.

Chapter 4, “Calibrating” contains calibration instructions for the module (if required).

Chapter 5, “Troubleshooting” contains explanations of self-tests and flowcharts for troubleshooting the module.

Chapter 6, “Returning and Replacing a U4164A Module or its cables” explains how to replace the module, its circuit board and cables and how to return these to Keysight Technologies.

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Keysight U4164A Logic Analyzer

Service Guide

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This chapter lists the accessories and some of the specifications and characteristics for testing and servicing the U4164A logic analyzer.

KEYSIGHT TECHNOLOGIES

Accessories

One or more of the following accessories, sold separately, are required to set up and operate the U4164A logic analyzer module for testing and servicing it.

Probes, Cables, and Accessories

Refer to the U4164A Data Sheet (5992-1057EN) on www.keysight.com to get a list of supported interposers, probes, and cables for U4164A. Details of these interposers, probes, and cables are in their respective user guides available on www.keysight.com.

Chassis and software

The U4164A logic analyzer requires:

- An AXIe chassis such as an M9502A or M9505A Keysight AXIe chassis that provides slots for installing the U4164A module.
- A host PC which is a laptop or a desktop PC with PCIe or USB interface. The host PC connects to the Keysight AXIe chassis via PCIe/USB interface and is used to host all the required software components of the U4164A module for configuring, controlling, and using this module.
- Keysight Logic Analyzer software version 06.20 or higher to configure, control, and use the U4164A module.

Refer to the *AXIe based Logic Analysis & Protocol Test Modules Installation Guide* to learn more about AXIe chassis, host PC, and the Logic Analyzer software installation.

Specifications

The specifications are the performance standards against which the product is tested.

U4164A Logic Analyzer State Speed Options	
State Speed Option	**Maximum State Data Rate**
Option 02G (spec)	2.5 Gb/s on 136 channels per U4164A, using either or both edges of clock (spec) 4 Gb/s on 68 channels per U4164A, clocking on either edge of the clock (typ)
Option 01G (spec)	2.5 Gb/s on 136 channels per U4164A, using both edges of clock (spec) 2.8 Gb/s on 68 channels per U4164A, clocking on either edge of the clock (typ)
Option 700	1.4 Gb/s on 136 channels using both edges of clock (spec)
Standard Speed (base)	700 Mb/s on 136 channels using both edges of clock (spec)

Characteristics

For a full listing of all specifications and characteristics, see the *Keysight U4164A Logic Analyzer Data Sheet,* literature part number 5992-1057EN available on Keysight's web site (www.keysight.com).

2 Preparing for Troubleshooting or Performance Testing

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This chapter provides instructions for preparing the U4164A logic analyzer module for troubleshooting or servicing it.

Operating Environment

The operating environment specifications are listed in the *Keysight U4164A Logic Analyzer Data Sheet,* literature part number 5992-1057EN available on Keysight's web site (www.keysight.com).

Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20°C to +35°C (+68°F to +95°F)

Humidity: 20% to 80% non-condensing

To set up the U4164A module

To set up the U4164A module for troubleshooting/servicing, you first need to install it in one of the slots of the AXIe chassis. Then connect the chassis to the host PC via a PCIe/USB link. On the host PC, install the Logic and Protocol Analyzer (6.20 or higher) application to configure and control the U4164A module. Connect the U4164A module to a probe and appropriate pod connector cables.

You can find the detailed instructions for configuring and installing the U4164A module into the AXIe chassis in the *AXIe based Logic Analysis & Protocol Test Modules Installation Guide*.

To test the U4164A module

The U4164A logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify logic analyzer's performance with the specifications, see "Testing U4164A Performance" on page 19.
- If you require a test to verify correct module operation, see "To run the self tests" on page 58.
- If the module does not operate correctly, see "Troubleshooting" on page 53.

To clean the module

- With the AXIe chassis turned off and unplugged, use a cloth moistened with a mixture of mild detergent and water to clean the front panel of the module.
- Do not attempt to clean the module's circuit board.

3 Testing U4164A Performance

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This chapter provides information on how to test the performance of the U4164A logic analyzer module against the specifications listed on page 13.

To ensure the U4164A logic analyzer module is operating as specified, software tests (self-tests) and a manual performance test is done. The logic analyzer is considered performance-verified if all of the software tests and the manual performance test have passed.

The specifications for the U4164A module define a maximum state data rate at which data can be acquired in state mode. The manual performance test (maximum state data rate test) verifies that the logic analyzer meets these specifications.

AXIe Chassis

You must test the U4164A logic analyzer module in a M9502A or M9505A AXIe chassis.

Test Strategy

Only specified parameters are tested. Specifications are listed on page 13. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specifications. No attempt is made to determine performance which is better than specifications. Not all channels of the logic analyzer will be tested; a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

NOTE **A U4164A module that is licensed with the Base state clock option, Option 700, Option 01G, or a memory option lower than 4M needs to be tested at a Keysight Service Center. The Service Center has the capability to test the module at up to the 2.5Gb/s state speed and 4M memory depth to ensure that the calibration will remain valid even after upgrading it to the -02G license or -400 license.**

Eye Scan is used to adjust the sampling position on every channel. Eye scan must be used to achieve maximum state data rate performance.

The 2.5 Gb/s state logic analyzer will be tested. All eight pods will be tested, one pod at a time.

The logic analyzer acquires data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

One-card Module

To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module

To perform a complete test on a multi-card module, perform the self-tests with the cards connected. Then, remove the multi-card module from the chassis and configure each card as a one-card module. Install the one-card modules into the chassis and perform the performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into their original multi-card module configuration, reinstall into the chassis and perform the self-tests again. These steps are necessary to ensure that the clocks are tested on each module.

Instructions for removing and installing the module can be found in the installation guide for the chassis or the U4164A module.

If you don't have the installation guide for your U4164A module, you can find the latest version on the Internet at www.keysight.com.

Test Interval

Test the performance of the U4164A module against its specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is provided in this chapter. You may want to make copies of the form, and fill-in a copy each time you test the module.

Test Equipment

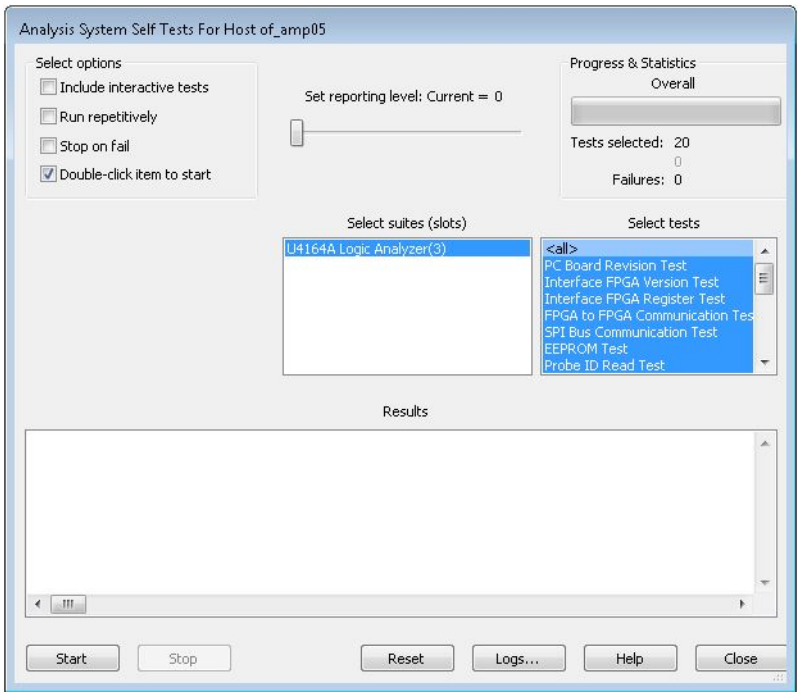
A list of the recommended test equipment is provided. You can use any equipment that satisfies the specifications given. However, the instructions are written with the presumption that you are using the recommended test equipment.

Perform the Self-Tests

Once you have connected all the hardware components for the U4164A module and created a logical module for U4164A in the Keysight Logic Analyzer application, you are ready to run the self-tests on U4164A.

1 Before performing the self- tests, disconnect all probes from the logic analyzer.

2 Select **Help**->**Self-Test..**. from the main menu. The **Analysis System Self Tests** window appears.



3 From the **Select suites** list, select the option displayed for U4164A. Then, select **All** from the **Select tests** list.

4 Select **Start** to start a complete module self-test. The progress of the self tests is displayed in the **Results** area of the window.

5 When the self-tests are complete, check the **Results** window to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to "To use the flowcharts" on page 54.

6 Select the **Close** button to close the **Analysis System Self Tests** window.

7 If all self- tests pass, then record "PASS" in the "Logic Analysis System Self-Tests" section of the Performance Test Record (page 48).

Equipment Required for the Performance Test

The following equipment is required for the performance test procedure.

Table 1 Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥1275 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Keysight 81134A or equivalent
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, δV=250 mV.) Required for 81134A or 8133A opt. 003.	Keysight 15435A
Flying Lead Probe Set (Qty 2)	A combination of U4201A & E5382A can be used.	Keysight U4203A
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	no substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 23

Assemble the SMA/Flying Lead Test Connectors

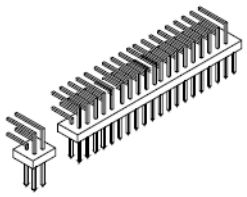
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the four required test connectors.

Table 2 Materials Required for SMA/Flying Lead Test Connectors

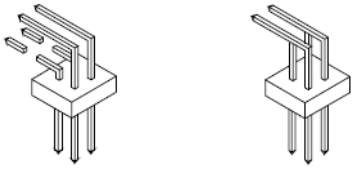
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 8)		Emerson 142-0701-801 (see www.emersonconnectivity.com)
Pin Strip Header (Qty 1, which will be separated)	0.100" X 0.100" Pin Strip Header, right angle, pin length 0.230", two rows, 0.120" solder tails, 2 X 40 contacts	3M 2380-5121TN or similar 2- row with 0.1" pin spacing
SMA 50 ohm terminators (Qty 4)	Minimum bandwidth 2 GHz	Emerson 142-0801-866 50 ohm Dummy Load Plug or similar
SMA m-m adapter (Qty 4)		Emerson 142-0901-811 SMA Plug to Plug or similar

1 Prepare the pin strip header:

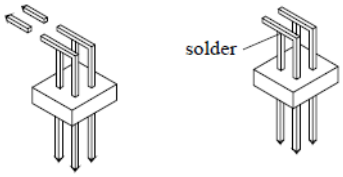
a Cut or cleanly break a 2 x 2 section from the pin strip.



b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.



c Trim about 2.5 mm from the outer leads.

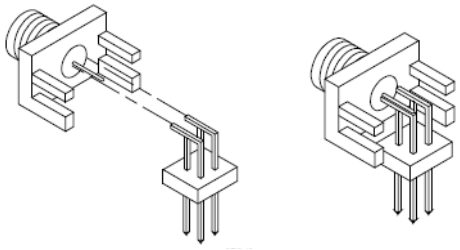


d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

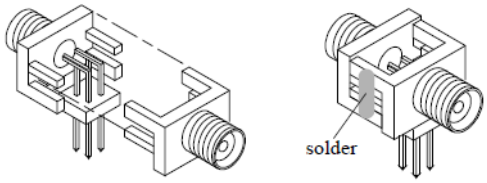
b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.



3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.



c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

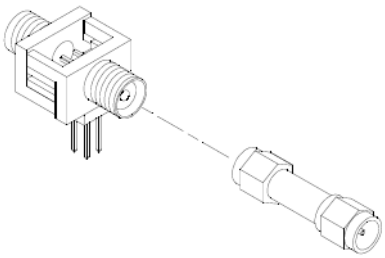
a Ensure that the following four points have continuity between them: The two pins on the left side of the pin strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

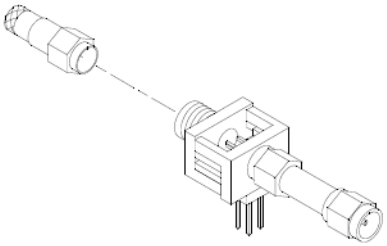
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

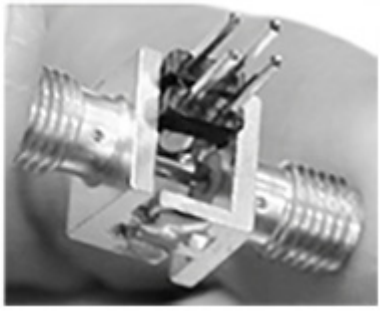
a Attach an SMA m-m adapter to one end of each of the four SMA/Flying Lead test connectors.



b Attach a 50 ohm terminator to the other end of the four SMA/Flying Lead test connectors.



c The finished test connector is shown in the pictures below.

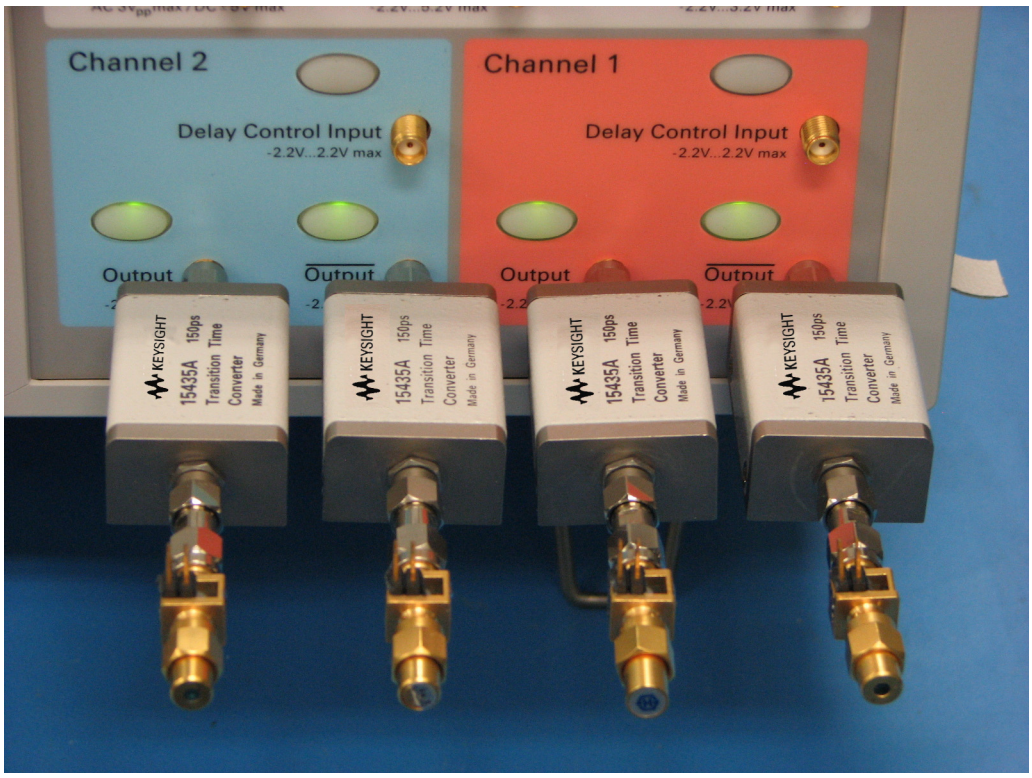


Set Up the Test Equipment

This section explains how to set up the test equipment for the maximum state data rate test.

1 Connect Transition Time Converters (if required) to each of the four outputs of the pulse generator: Channel 1 OUTPUT, Channel 1 OUTPUT (not), Channel 2 OUTPUT, Channel 2 OUTPUT (not).

2 Connect the four SMA/Flying Lead test connectors (see "Assemble the SMA/Flying Lead Test Connectors" on page 23) with 50 ohm terminators to the Transition Time Converters on the 4 pulse generator outputs. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)



3 Turn on the Pulse Generator. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

4 Load the default configuration into the 81134A Pulse Generator.

- Select Main
- Hit Recall
- Press 0

5 Setup the pulse generator according to the following.

a Set the frequency of the pulse generator:

In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to:

- Base Option: Temporarily License the module to full speed and test at 1250 MHz plus 0.81% (1260 MHz)

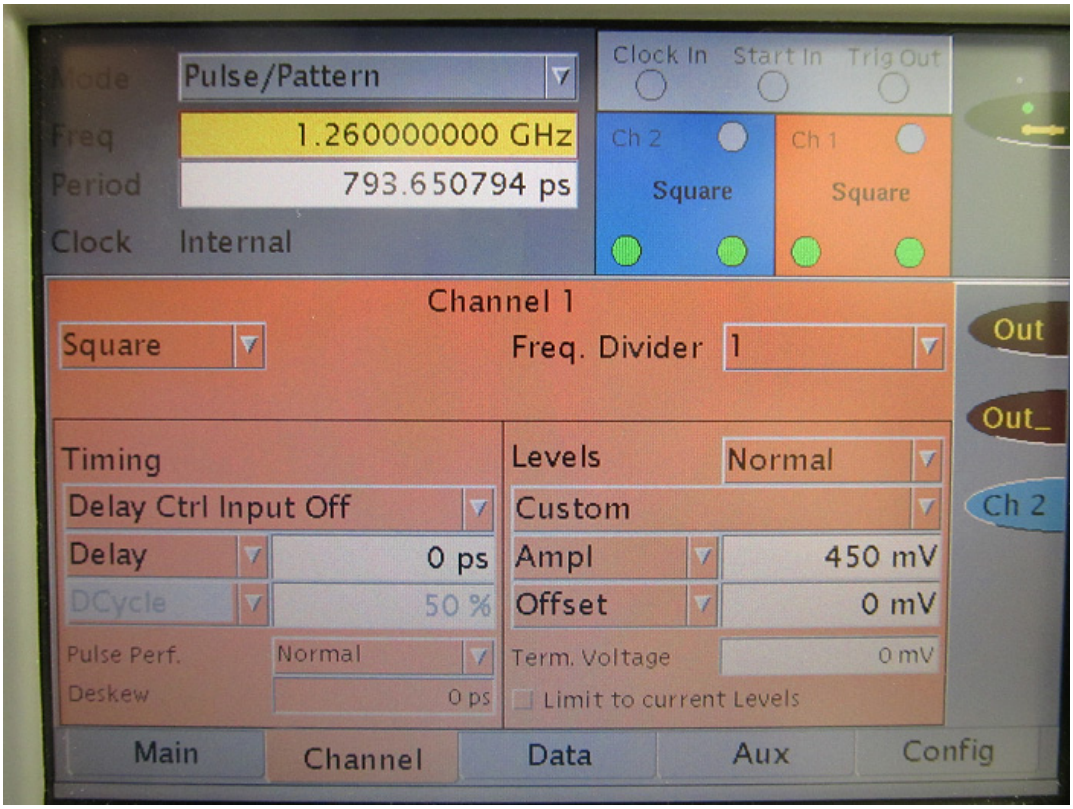
- Option 700: Temporarily license the module to full speed and test at 1250 MHz plus 0.81% (1260 MHz)
- Option 01G: Temporarily license the module to full speed and test at 1250 MHz plus 0.81% (1260 MHz)
- Option 02G: 1250 MHz plus 0.81% (1260 MHz)

This includes the frequency uncertainty of the pulse generator, cabling, and a test margin. If you are using an 81134A pulse generator, the frequency accuracy is ±0.005% of setting.

b Set the rest of the pulse generator parameters to the values shown in the following tables.

Table 3 81134A Pulse Generator Setup

Main	Channel 1	Channel 2
Mode: Pulse/Pattern	Mode: Square ÷ 1	Mode: Square ÷ 1
Freq: set in previous step	**Timing**	**Timing**
Clock Internal	Delay Ctrl Input Off	Delay Ctrl Input Off
	Delay 0 ps	Delay 0 ps
	Pulse Perf: Normal	Pulse Perf: Normal
	Deskew: 0 ps	Deskew: 0 ps
	Levels: Normal, Custom	**Levels: Normal, Custom**
	Ampl: 450 mV	Ampl: 450 mV
	Offset: 0 mV	Offset: 0 mV
	Term Voltage: 0 mV	Term Voltage: 0 mV
	Limit to current Levels: unselected	Limit to current Levels: unselected
	Output: Enable (LED on)	Output: Enable (LED on)
	Output: Enable (LED on)	Output: Enable (LED on)

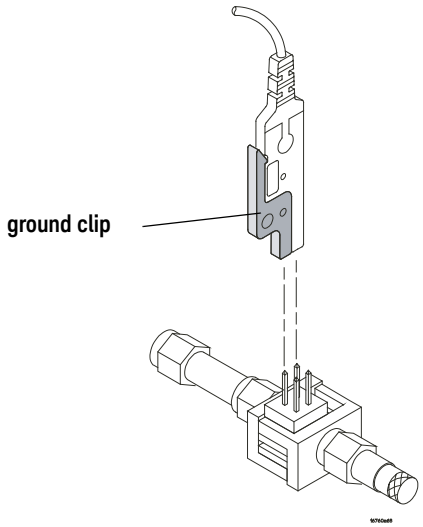

Pulse/Pattern
Freq
1.260000000 GHz
Period
793.650794 ps
Clock
Internal
Clock In
Start In
Trig Out
Ch 2
Square
Ch 1
Square
Channel 1
Square
Freq. Divider
1
Out
Out_
Ch 2
Timing
Delay Ctrl Input Off
Delay
0 ps
DCycle
50 %
Pulse Perf.
Normal
Deskew
0 ps
Levels
Normal
Custom
Ampl
450 mV
Offset
0 mV
Term. Voltage
0 mV
Limit to current Levels
Main
Channel
Data
Aux
Config

Connect the Test Equipment

Connect the Logic Analyzer Pod to the Pulse Generator

1 Connect one U4203A Flying Lead Probe Set to Pods 1/2 of the U4164A module.

2 Connect the Pod 1 U4203A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT.



NOTE On all connection be sure to use the black ground clip (supplied with the U4203A Flying Lead Probe Set) and orient the leads so that the black clip is connected to one of the SMA/Flying Lead connector's ground pins!

3 Connect the Pod 1 U4203A Flying Lead Probe Set's CLK (NOT) lead to the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT (NOT). Again, be sure to use the black ground clip and orient the leads so that the black clip is connected to ground.

4 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT.

5 Connect the Pod 1 U4203A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT (NOT).


81134A
Clock Input
Start Input
Trigger Out
Channel 2
Delay Control Input
Output
KEYSIGHT
15435A

Test the U4164A Module

The following sections explain how to test the maximum state data rate.

1 Record the logic analyzer's model and serial number in the Performance Test Record (see page 48). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the “Test Equipment Used” section of the Performance Test Record.

3 Turn on the AXIe chassis.

NOTE **Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.**

a Plug in the power cord to the power connector on the rear panel of the AXIe chassis.

b Press the ON/Standby button on the front panel of the chassis to power on the logic analyzer.

4 After the AXIe chassis is fully booted, power on the host PC if it is not part of the AXIe chassis.

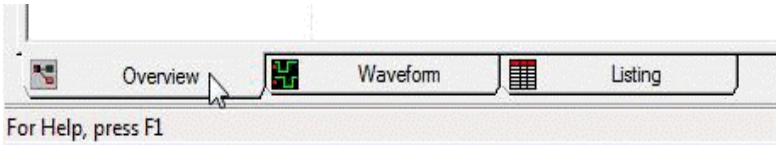
5 Start the Keysight Logic and Protocol Analyzer application if it is not started already.

Configure the Logic Analysis System

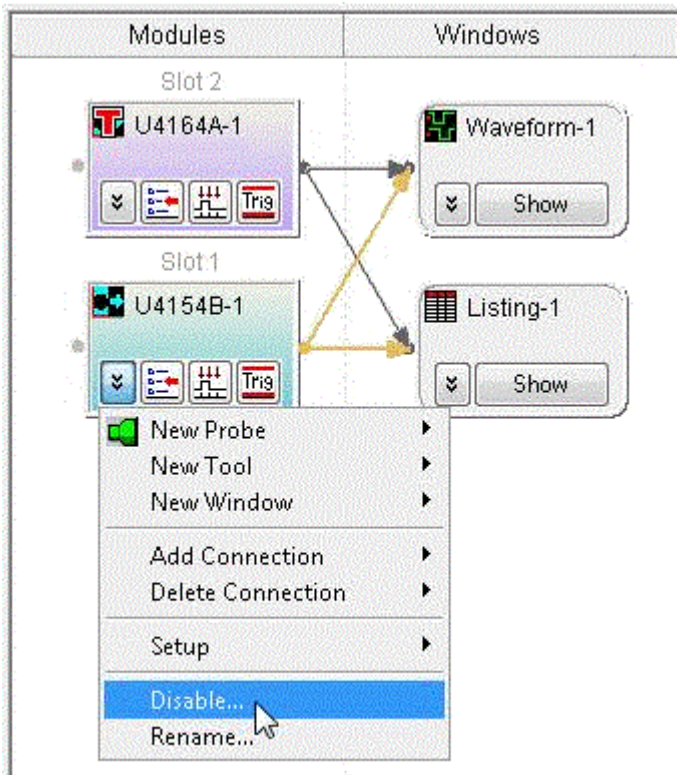
1 In the *Keysight Logic and Protocol Analyzer* application, choose **File→New**. This puts the logic analysis system into its initial state.

2 Disable all logic analyzers other than the analyzer under test.

a Select the **Overview** tab at the bottom of the main window.

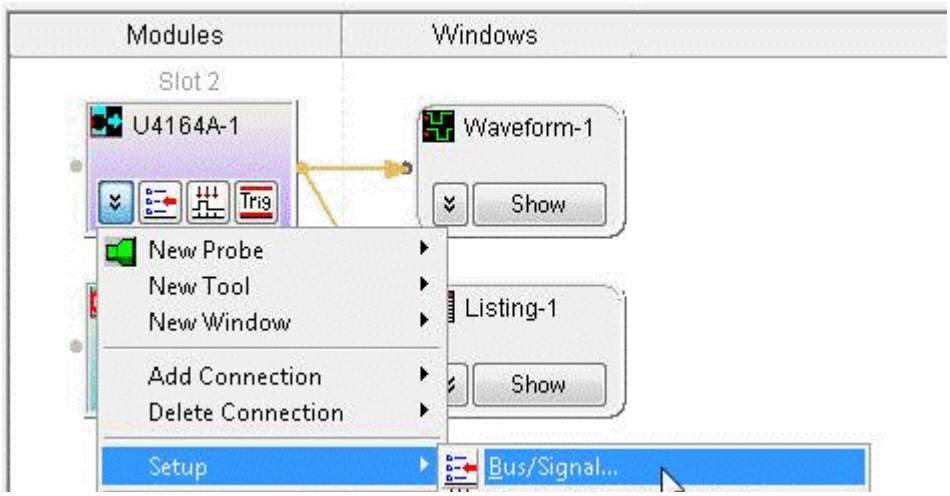


b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.



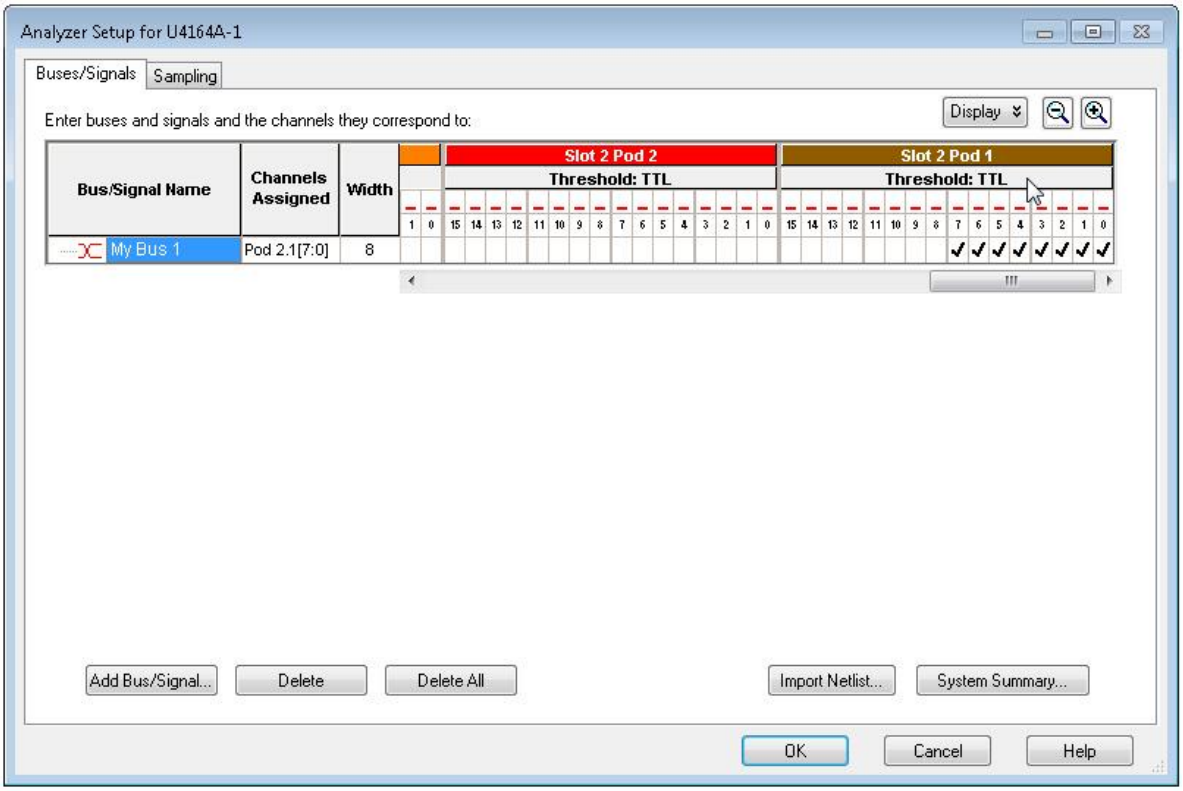
3 Set up the bus and signals:

a In the Overview window, select **Setup→Bus/Signal...** from the logic analyzer's drop-down menu.



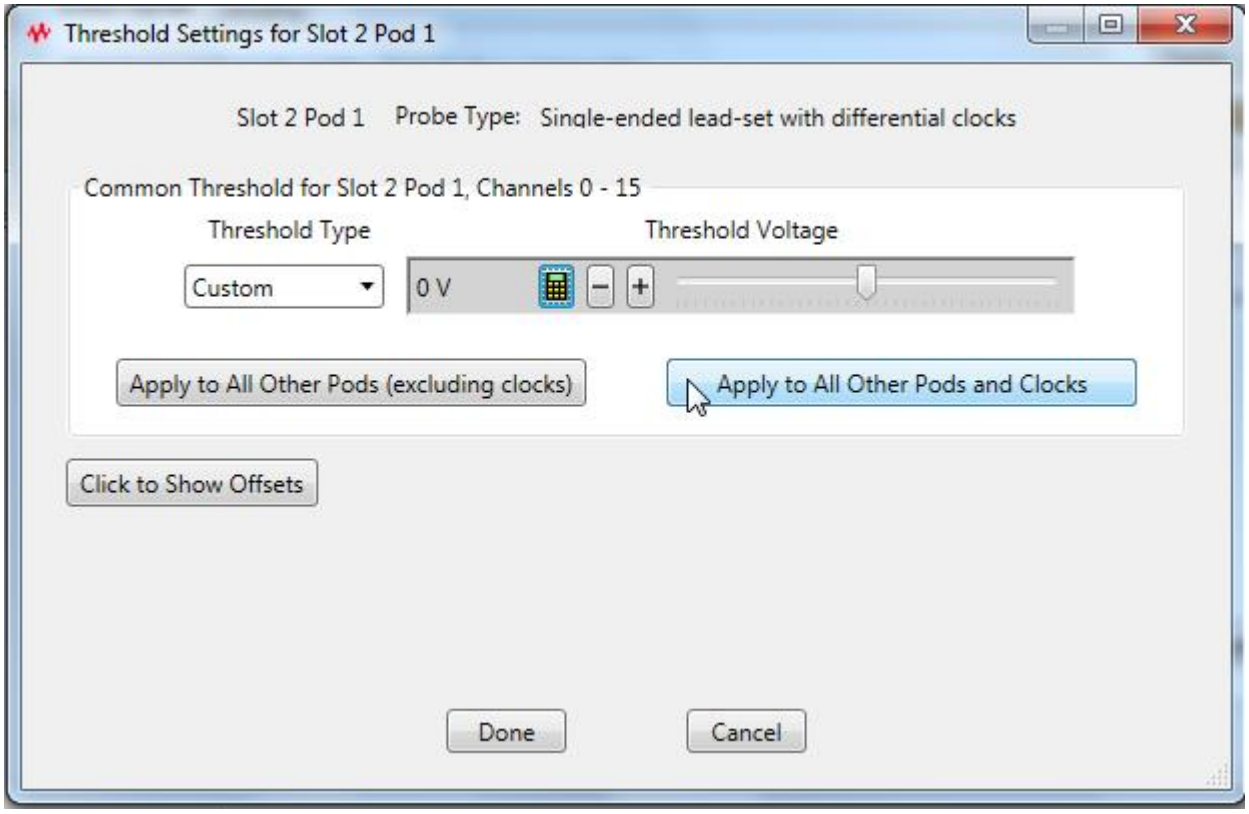
NOTE The U4203A probe must be connected to the logic analyzer pod as described on page 29.

b In the Analyzer Setup window, choose the **Threshold** button for Pod 1.

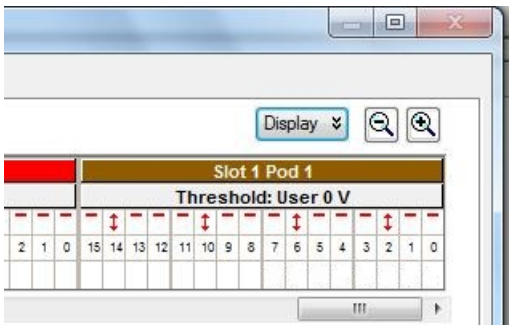


The **Threshold Settings** window appears.

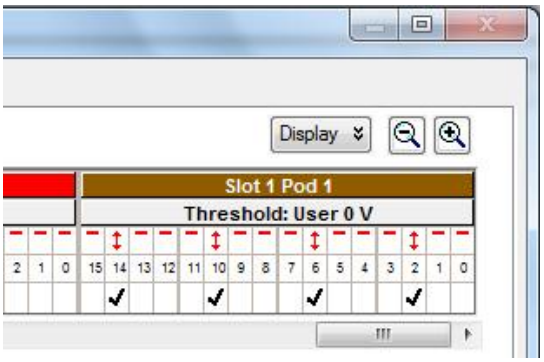
c Set the threshold value for Pod 1 of the logic analyzer to **0 V**. Click **Apply to All Other Pods and Clocks**. Then, click **Done** to close the dialog.



d The activity indicators now show activity on the channels that are connected to the pulse generator. Un-assign all channels. You can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks.

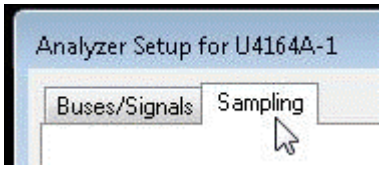


e Click to select channels 2, 6, 10, and 14 as shown in the picture above.

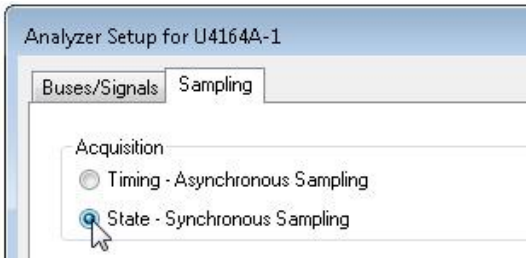


4 Select the State sampling mode and set the State Clock options:

a Select the **Sampling** tab of the Analyzer Setup window.



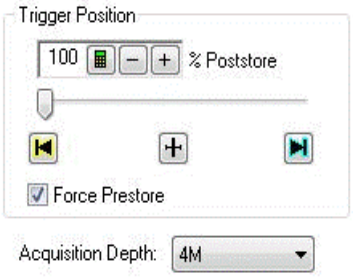
b Select **State - Synchronous Sampling**.



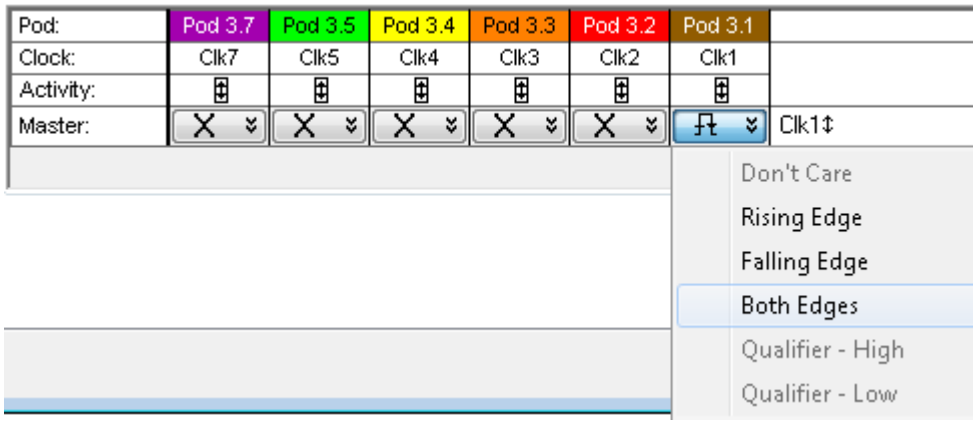
5 Set the trigger position and acquisition memory depth:

a Set the Trigger Position to **100% Poststore**.

b Set the Acquisition Depth to **4M**.



c Set Clk1 to **Both edges** clocking. The following screen displays this state clock setting.



6 Hit **OK** to close the setup window.

Determine maximum clock rate

1 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

2 Click the **Run Repetitive** tool-bar button to start a repetitive run on the logic analyzer for acquiring data repeatedly.

Acquired data will start appearing in the Listing window.

3 Start increasing the frequency on the pulse generator by 1 MHz increments while simultaneously observing the logic analyzer data acquisition status.

4 When the logic analyzer displays an error that the data could not be displayed, decrease the pulse generator frequency by 1 MHz.

5 Close the displayed error dialog by clicking **OK**.

6 Click **Run Repetitive** .

7 Wait for logic analyzer to complete 100 acquisitions at the new pulse generator frequency without displaying any error. If an error is displayed, decrease the pulse generator frequency by 1 MHz and then again wait for 100 acquisitions at this new frequency without any error. Repeat this step until you get 100 acquisitions without any error display.

8 Click the **Stop** tool-bar button to stop the data acquisition.

Determine PASS/FAIL for the Pulse Generator Frequency test

If you get 100 acquisitions without any error display at a pulse generator frequency (including uncertainty) greater than *1250 MHz*, then the logic analyzer passes this portion of the test. For example, a frequency of *1270 MHz - 0.81% uncertainty = 1259.7 MHz* indicates a PASS result for the test (results should be approx. 1270 MHz). Record PASS/FAIL result of this test in the "**Pulse Generator Frequency Test**" section of the Performance Test Record (page 48).

NOTE

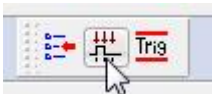
If any of tests described later in this chapter fail, decrease the pulse generator frequency by 1 MHz and wait for logic analyzer to complete 100 acquisitions at this new pulse generator frequency without displaying any error. Repeat this step until you get 100 acquisitions without any error display.

Final pulse generator frequency

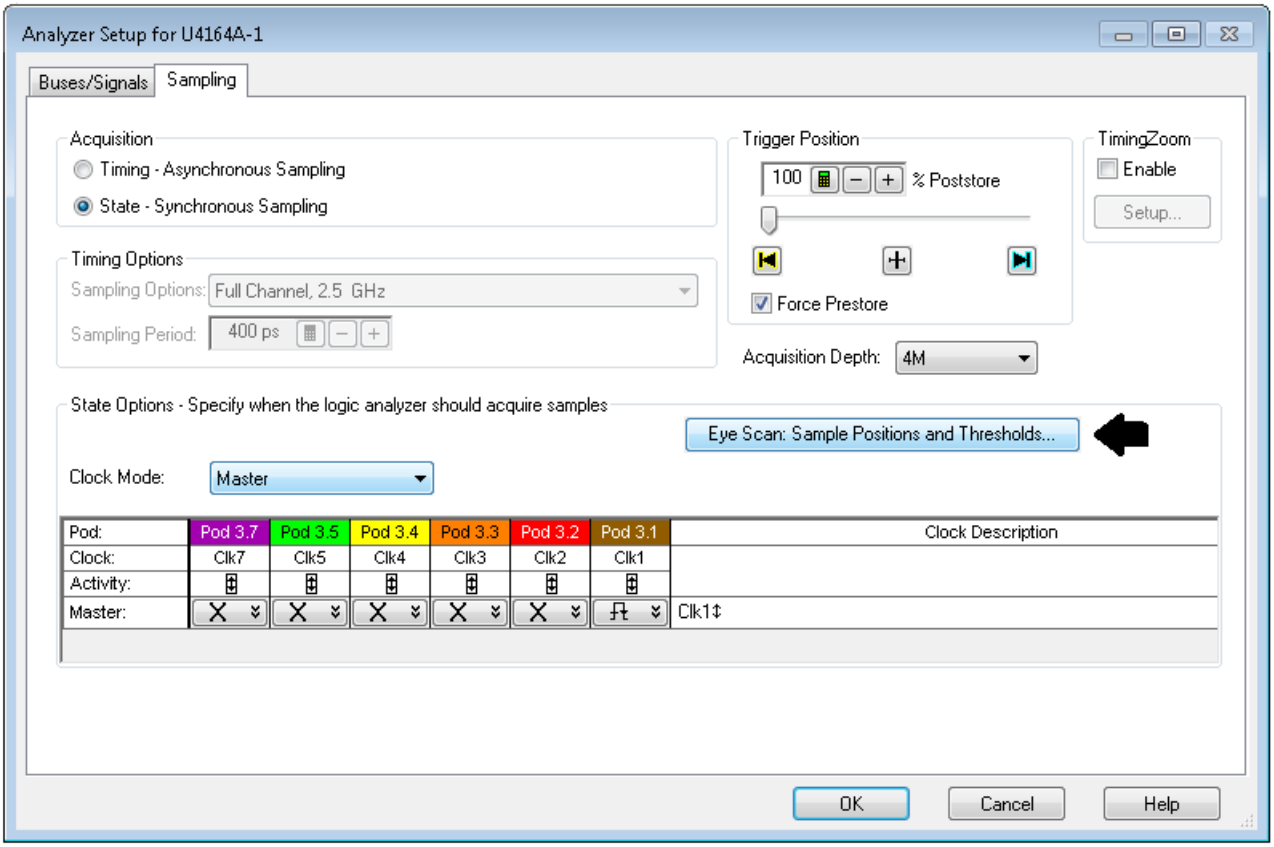
If the remaining tests described in this chapter PASS, record the final pulse generator frequency in the "**Final Pulse Generator Frequency**" section of the Performance Test Record (page 48). Recording this final frequency provides a traceable measurement that is expected to be unique for each U4164A Logic Analyzer module.

Adjust sampling positions using Eye Scan

1 Open the sampling setup window.

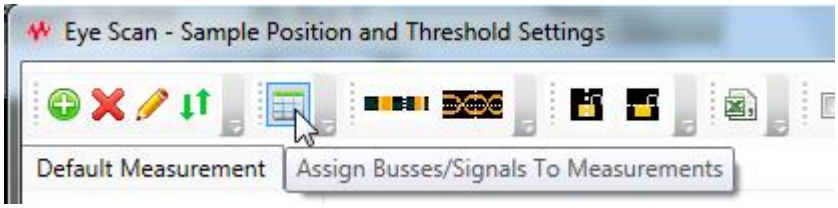


2 Select the **Eye Scan: Sample Positions and Thresholds...** button.

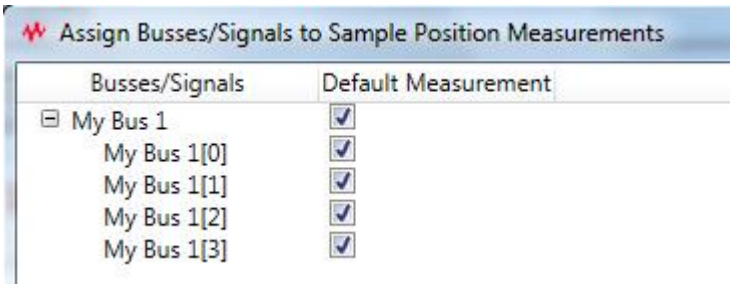


The Eye Scan - Sample Positions and Threshold Settings dialog will appear.

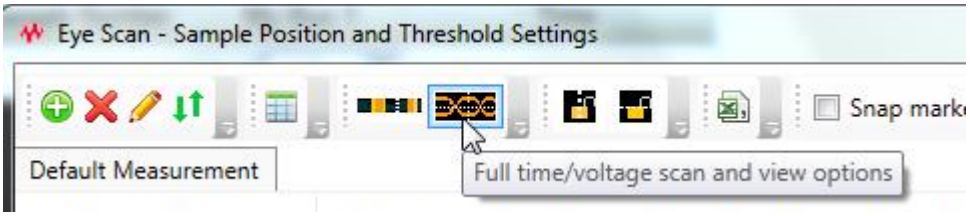
3 Select the **Assign Busses/Signals** Dialog.



4 In the **Busses/Signals** section of the dialog, ensure that the check box next to “My Bus 1” is checked and the 4 data bits 0-3. Hit **OK**.



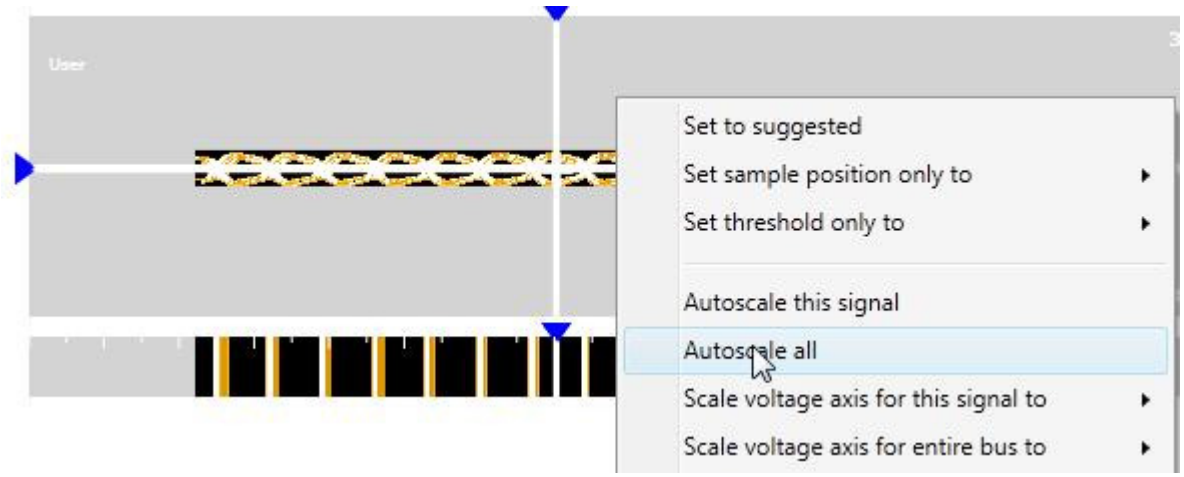
5 Select the **Full time/voltage scan** dialog box.



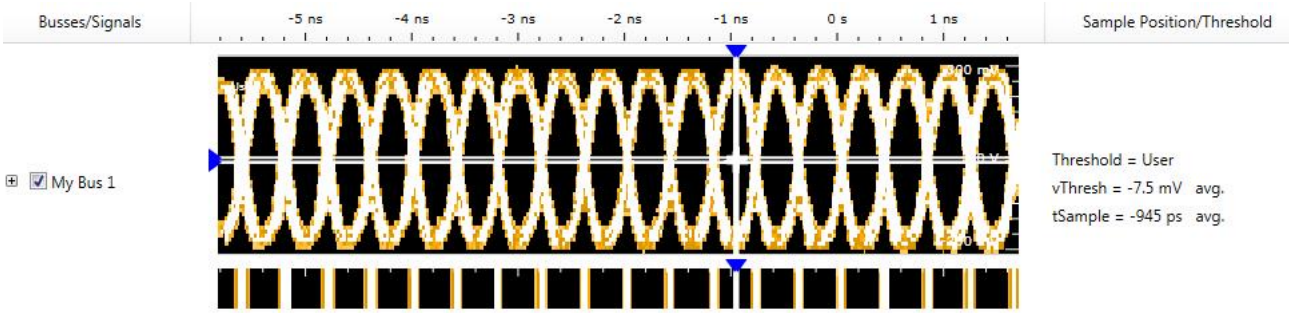
6 In the dialog box, set **Do full time/voltage scan** and **Show time/voltage scan**.

7 Run Eye Scan by hitting the **Run This Measurement** button.

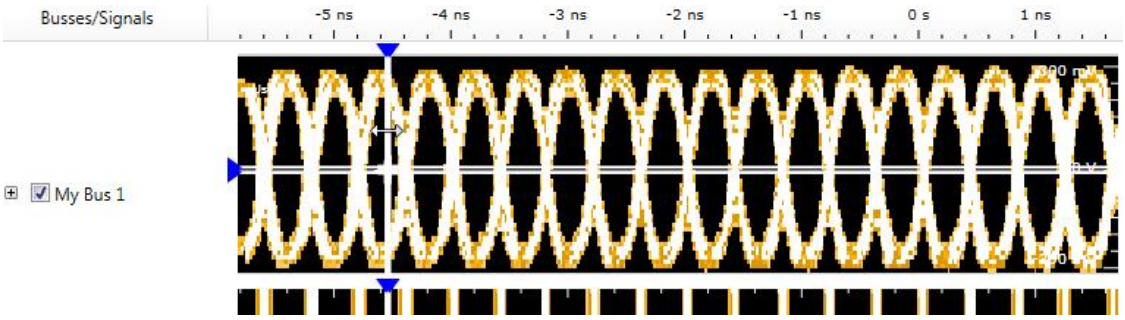
8 If the scan does not fill the scan area, right click in the scan area and select **Autoscale all**.



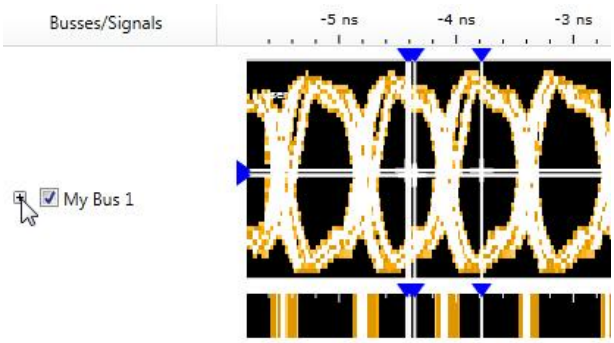
The waveform should now fill the Eye Scan area.



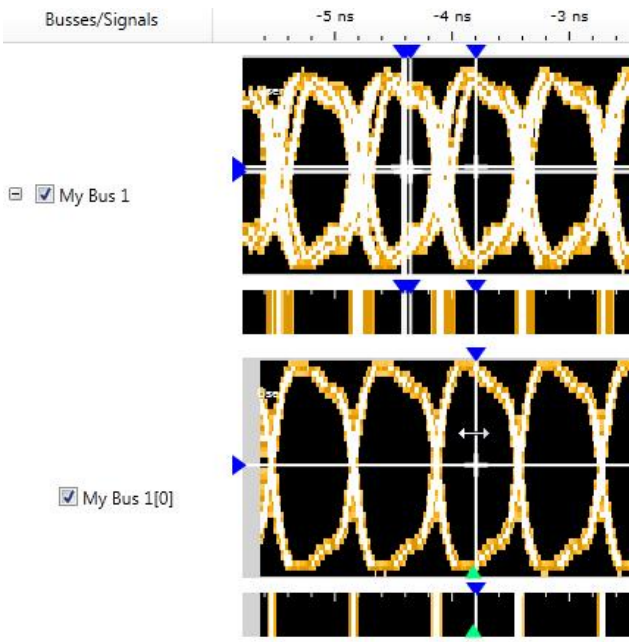
9 Move the sample position of all 4 data bits into the Eye nearest -4.5ns.
Using the mouse grab the vertical lines and move them into the correct eye.



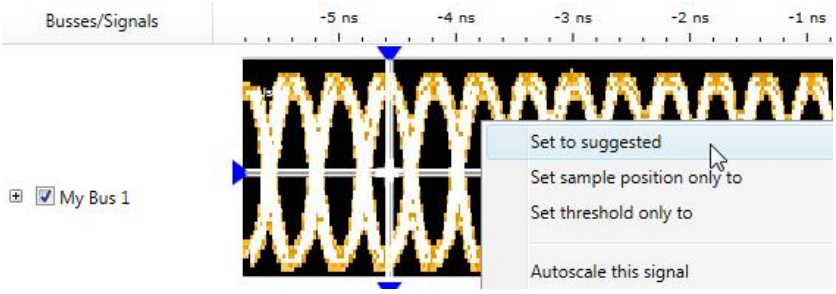
10 If all sample positions are not in the same eye. Then hit the Plus sign to expand My Bus 1.



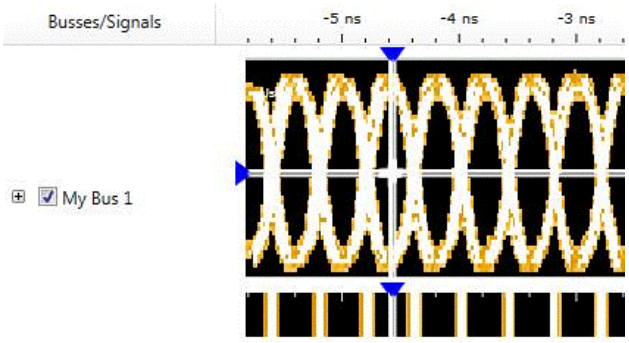
Use the mouse to grab the bits that are not in the eye near -4.5 ns. Drag them into the correct eye.



11 After all bit sample positions are in the correct eye. Right click in the My Bus 1 Scan area and select **Set to Suggested**.



12 After setting to suggested all bits should be centered in their own eye near -4.5 ns.



Test Pod 1

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests) Eye Scan Location

1. PASS/FAIL: If an eye exists near -4.5 ns for every bit, and Eye Scan places the sample position in the eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "**Eye Scan locates an eye for each bit**" section of the Performance Test Record (page 48).
2. If an eye does not exist near -4.5 ns for every bit or Eye Scan cannot place the blue bar in the eye, then the logic analyzer fails the test. Record the result in the "**Eye Scan locates an eye for each bit**" section of the Performance Test Record (page 48).

Close the Eye Scan and Analyzer Setup Windows

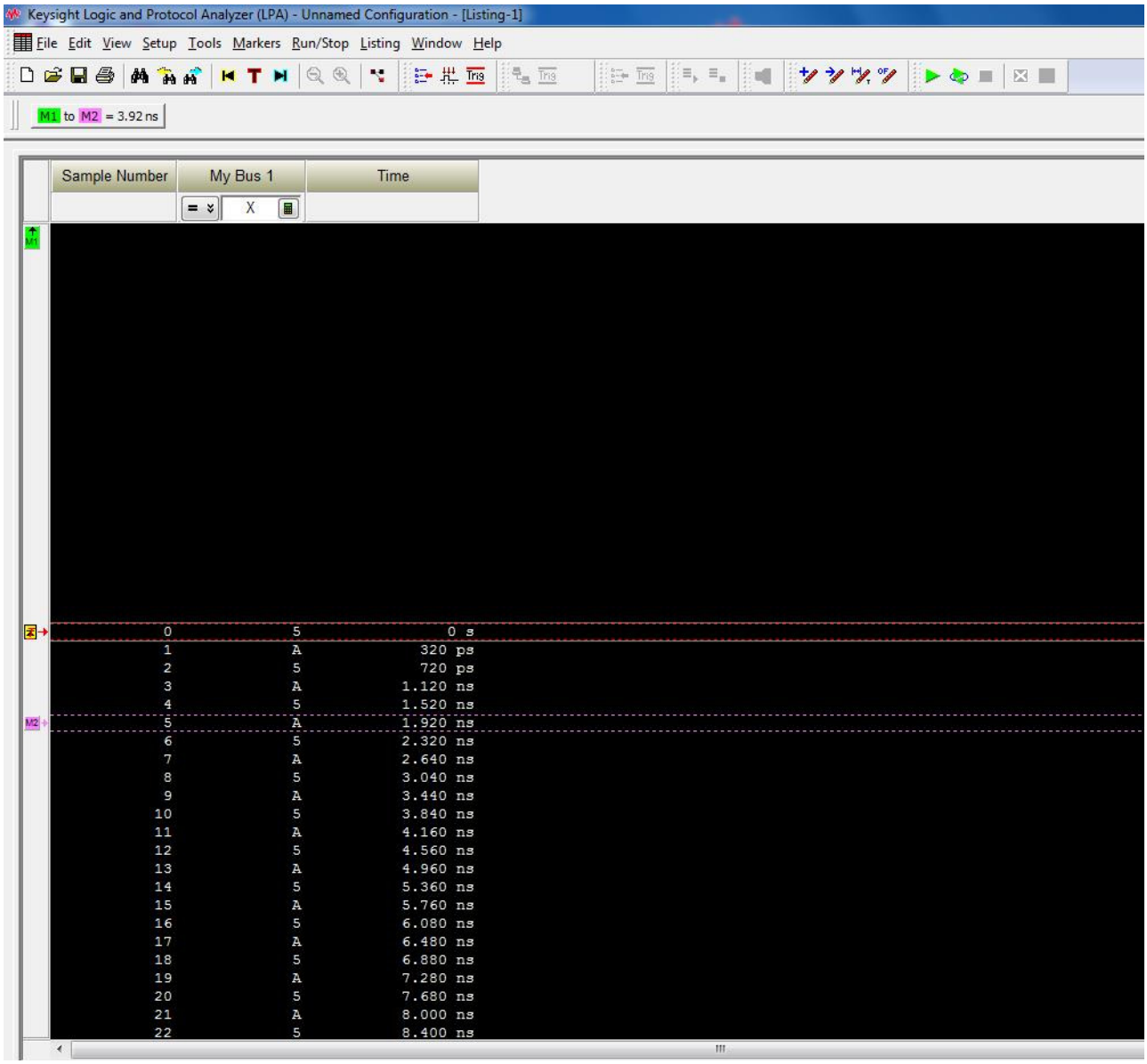
1. Select **OK** to close the Eye Scan - Sample Positions and Threshold Settings dialog.
2. Select **OK** to close the Analyzer Setup window.

Configure the markers

Data must be acquired before the markers can be configured. Therefore, you need to run the analyzer to acquire data.

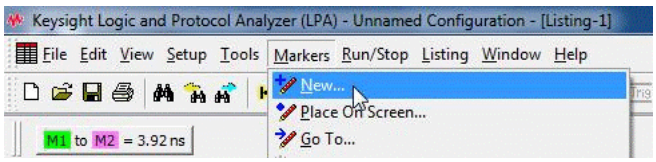
1. Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.
2. Select the Run icon  .

Data will appear in the Listing Window upon completion of the run.



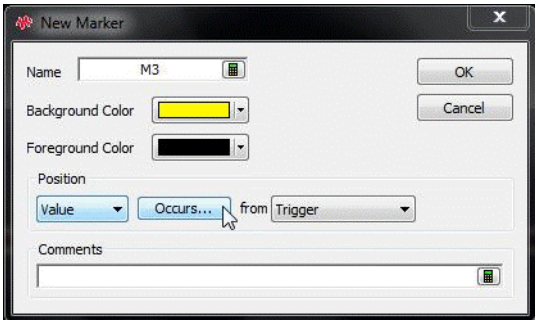
If the data values are not “A”s and “5”s, you may need to set the sampling positions in different eyes.

3 From the Main Menu, choose **Markers→New**.

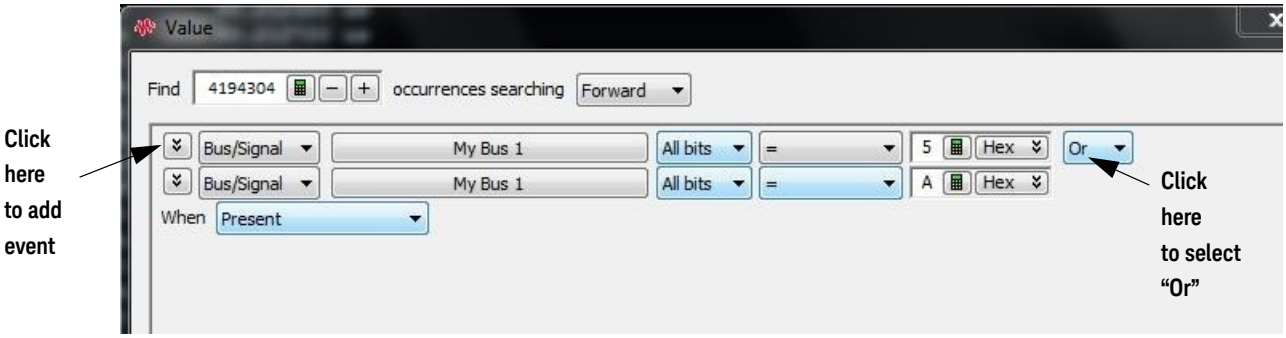


4 You can accept the default name for the new marker.

5 Change the Position field to **Value**.

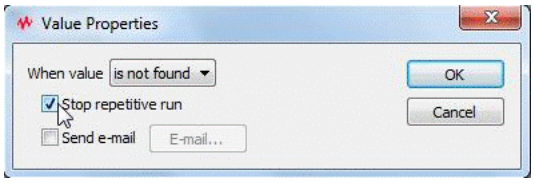


6 Select the **Occurs...** button and create the marker setup shown below.



7 In the Value window, select the **Properties...** button.

8 In the Value Properties window, select **Stop repetitive run** when value **is not found**.



9 Select **OK** to close the marker Value Properties window.

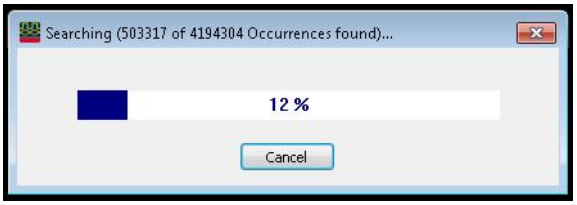
10 Select **OK** to close the marker Value window. The system will search the display for the occurrences specified.

11 Select **OK** to close the New Marker window.

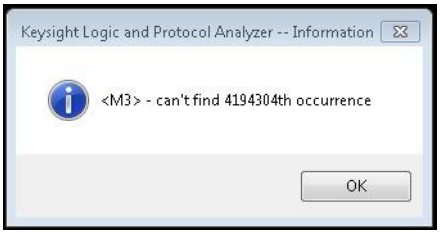
Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear.

1 Select the Run Repetitive icon  . Let the logic analyzer run for five runs (this should take about 2-3 minutes). The analyzer will acquire data and the Listing Window will continuously update.



If the “can’t find occurrence” window appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the “**Maximum State Data Rate**” section of the Performance Test Record.

NOTE **Be sure that the black ground clip is making good contact with the ground pin on the test connector.**

2 After five runs, select the **Stop** button  to stop the acquisition.

If the “can’t find occurrence” window does not appear, then the analyzer passes the test. Record “Pass” in the “**Maximum State Data Rate**” section of the Performance Test Record.

Test Pod 2

1 Disconnect the U4203A Flying Lead Probe Set Pod1 from channel 2 of the 81134A pulse generator output (Bits 2, 6, 10, 14). Leave the Pod 1 clock connected to channel 1.

2 Connect the probe set from Pod 2 of logic analyzer to the pulse generator channel 2 outputs. (The clock input on Pod 1 remains the clock input when testing Pod 2.)

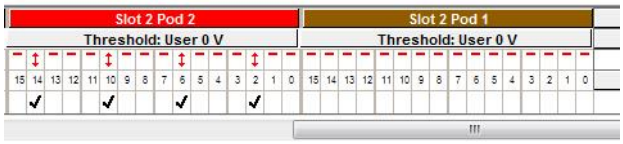
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

3 In the Overview window, select **Setup→Bus/Signal...** from the analyzer's drop-down menu**.**

4 Scroll to the right and unassign all Pod 1 bits.

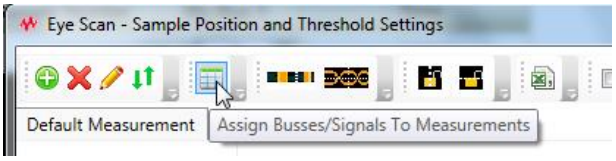
5 Set the Pod 2 threshold to 0 V (just as you did for Pod 1 on Set the threshold value for Pod 1 of the logic analyzer to).

6 Assign bits 2, 6, 10, and 14 of Pod 2.



7 Adjust the sampling positions using Eye Scan. Set sample position near -4.5 ns. Realign any stray channels if necessary.

In Eye Scan - Open **Assign Busses** and assign 4 bits to My Bus.



8 Determine pass or fail (1 of 2 tests) Eye Scan Location. See page 42.

9 Select **OK** to close the “Analyzer Setup” window.

10 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

11 Select the Run Repetitive icon  .

12 Determine pass or fail (2 of 2 tests). See page 45.

Test Pods 3

1 Disconnect the U4203A Flying Lead Probe Set Pod2 from channel 2 of the 81134A pulse generator output. Leave the Pod 1 clock connected to channel 1.

2 Connect a second U4203A to the Pod 3 / 4 connector on the Logic Analyzer frame.

3 Connect the probe set from Pod 3 of logic analyzer to the pulse generator channel 2 outputs. (The clock input on Pod 1 remains the clock input when testing other Pods.)

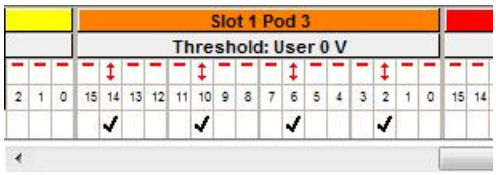
- Bits 2 & 10 to Channel 2 Output
- Bits 6 & 14 to Channel 2 Output (not)

4 In the Overview window, select **Setup Bus/Signal...** from the analyzer's drop-down menu.

5 Scroll to the right and unassign all Pod 2 bits.

6 Set the Pod 3 threshold to 0 V. Apply to All Other Pods and Clocks (just as you did for Pod 1 on Set the threshold value for Pod 1 of the logic analyzer to).

7 Assign bits 2, 6, 10, and 14 of Pod 3.



8 Adjust the sampling positions using Eye Scan. Set sample position near -4.5 ns. Realign any stray channels if necessary.

In Eye Scan - Open **Assign Busses** and assign 4 bits to My Bus.

9 Determine pass or fail (1 of 2 tests) Eye Scan Location. See page 42.

10 Select **OK** to close the "Analyzer Setup" window.

11 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

12 Select the Run Repetitive icon  .

13 Determine pass or fail (2 of 2 tests) occurrences. See page 45.

Other Pods

Repeat the above steps for testing pods 4 to 8. Upon completion, the logic analyzer is completely tested.

Conclude the State Data Rate Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a From the Main Menu, choose **File→Exit**. At the dialog "Do you want to save the current configuration?" select **No**.

b Disconnect all cables and adapters from the pulse generator.

Performance Test Record

LOGIC ANALYZER MODEL NO.: U4164A	
Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours
	Recommended next testing:

TEST EQUIPMENT USED
Pulse Generator Model No.
Pulse Generator Serial No.
Pulse Generator Calibration Due Date:

MEASUREMENT UNCERTAINTY
Clock Rate
Pulse Generator Frequency Accuracy: 81134A: ±0.005% of setting. Approx. Cabling Accuracy ±0.005% of setting. 0.81% = ±0.010% Uncertainty + 0.8% Test Margin.
Setting Base option: (should be tested to the Option 02G level at the service center) Option 02G: 1250 MHz + 0.81% = 1260 MHz

TEST RESULTS		
Logic Analysis System Self-Tests (Pass/Fail):		
Performance Test: Maximum State Data Rate:		
Pulse Generator Settings	Freq: Option 02G: 1250 MHz + 0.81% = 1260 MHz	
	Square wave.	
Pulse Generator Frequency Test (Pass/Fail)		
Final Pulse Generator Frequency		
Test Criteria	Test 1 of 2 Eye Scan locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):		
Pod 2 Results (pass/fail):		
Pod 3Results (pass/fail):		
Pod 4 Results (pass/fail):		
Pod 5 Results (pass/fail):		

TEST RESULTS
Pod 6 Results (pass/fail):
Pod 7 Results (pass/fail):
Pod 8 Results (pass/fail):

4 Calibrating

Calibration Strategy / 52

This chapter provides instructions for calibrating the U4164A logic analyzer.

Calibration Strategy

The U4164A logic analyzer does not require any periodic adjustments or calibration by the user to ensure operational accuracy.

However, Keysight recommends that performance of the U4164A logic analyzer be tested against its specifications at two-year intervals. This testing is required in order to obtain calibration certification.

You can refer to Chapter 3, “Testing U4164A Performance" to find detailed information on how to test the performance of the U4164A logic analyzer.

5 Troubleshooting

To use the flowcharts / 54
To run the self tests / 58
Self-Test Descriptions / 56
To exit the test system / 58
To test the cables / 59

This chapter provides instructions for troubleshooting a U4164A module that is not operating correctly.

The troubleshooting consists of flowcharts, self-test instructions, and a cable test.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for the U4164A module is the replacement of defective assemblies. You can return this module to Keysight Technologies for all service work, including troubleshooting. Contact your nearest Keysight Technologies Sales Office for more details.

CAUTION **Electrostatic discharge can damage electronic components. Use grounded wrist-straps and mats when you perform any service to this instrument or to the modules in it.**

To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the problem. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

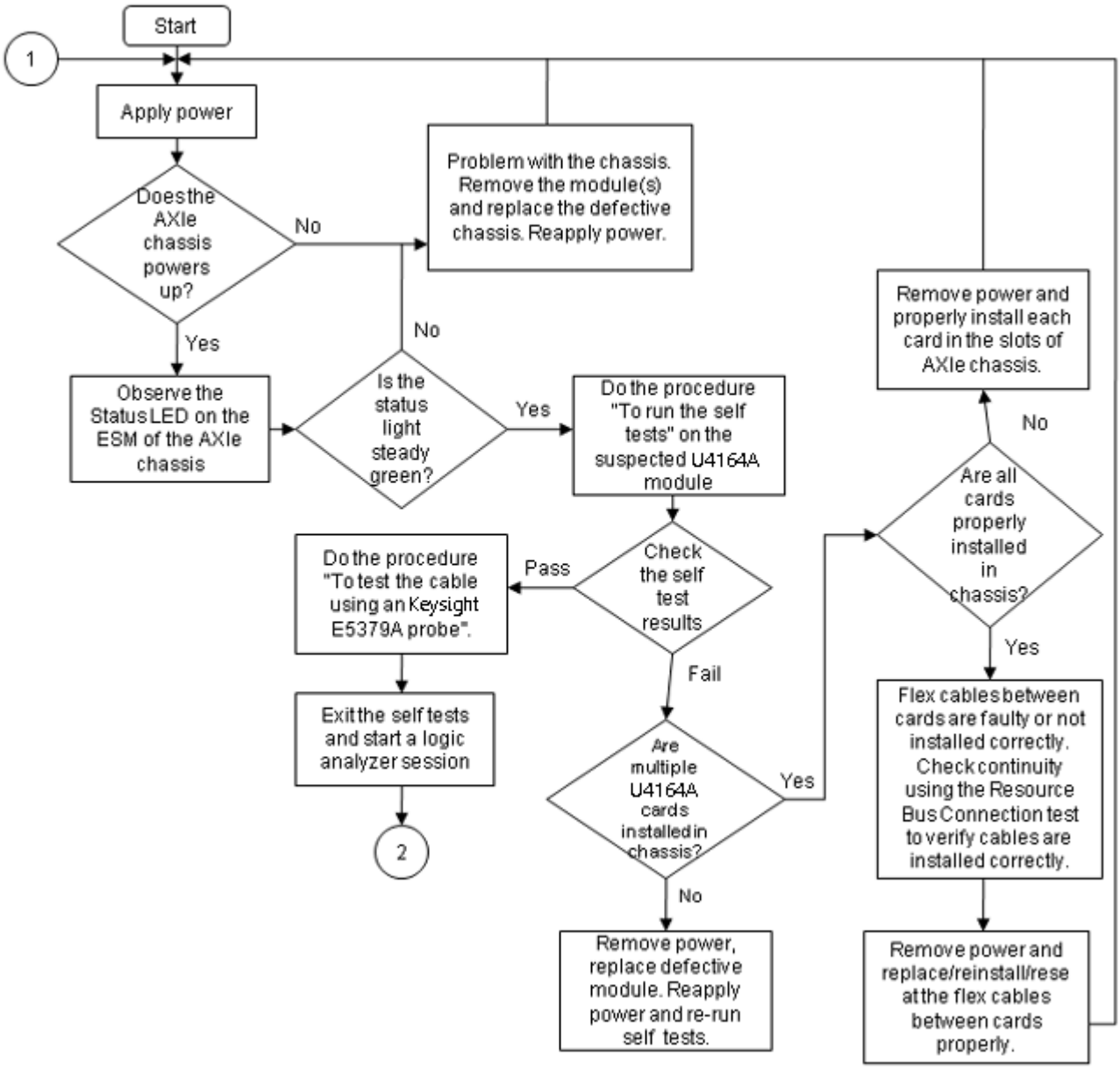


Figure 3 Troubleshooting Flowchart 1

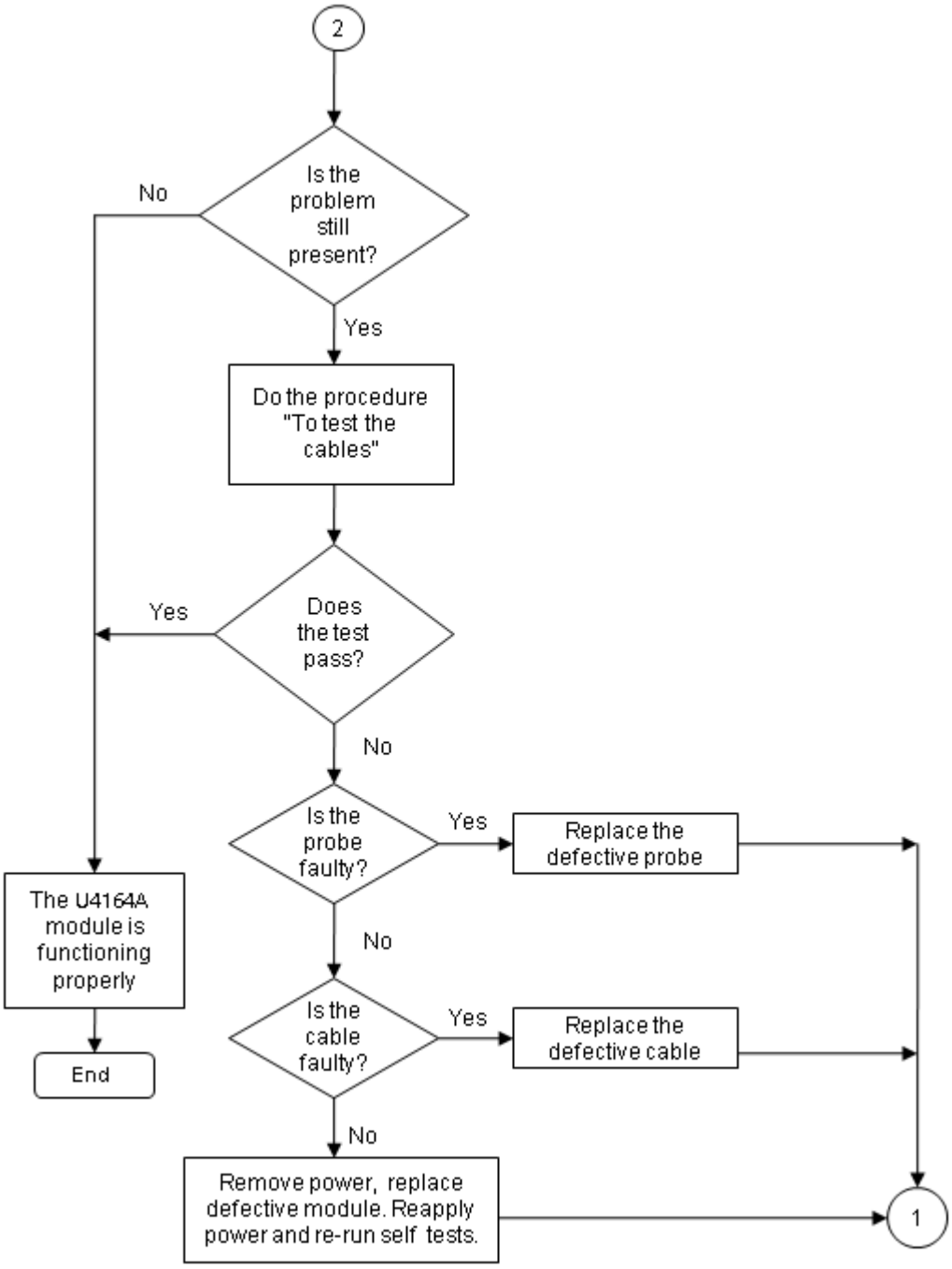


Figure 4 Troubleshooting Flowchart 2

Self-Test Descriptions

The self-tests for U4164A logic analyzer identify the correct operation of major functional areas in the U4164A module.

PC Board Revision Test

This tests that the FPGA is communicating with the backplane and that the board under test is a supported version.

Interface FPGA Version Test

This test verifies that the FPGA program is a version that the software can use. This is necessary because new features will be added to the U4164A that will require both new software and new FPGA bits.

Interface FPGA Register Test

The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. The FPGA must be working before any of the other circuits on the board will work. Also, the FPGA generates the board ID code that is returned to identify the module and slot.

FPGA to FPGA Communication Test

This test is only run if there are two or more U4164A logic analyzer cards installed in a chassis and connected together with the flex cables. The purpose of this test is to verify that the FPGAs can drive and receive the signals correctly.

SPI Bus Communication Test

The purpose of this test is to verify communications over the SPI bus from the Interface FPGA to various devices attached to the SPI bus.

EEPROM Test

The purpose of this test is to verify:

- The address and data paths to the EEPROM.
- That each cell in the EEPROM can be programmed high and low.
- That individual locations can be independently addressed.
- The EEPROM can be block erased.

Probe ID Read Test

The purpose of this test is to verify that the Probe ID values can be correctly read and to verify the functionality of the Digital to Analog Converter by testing the two Probe ID DAC outputs at various voltage levels.

Chip Registers Read/Write Test

The purpose of this test is to verify that each bit in each register of the Analysis chip can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

Freq Synth Lock Detect Test

This test determines if all the voltage-controlled oscillators (VCOs) are working properly.

Acquisition Chip BIST Test

Tests the Timing Zoom memory and other internal memories on the acquisition chip.

Resource Bus Connection Test

This test is only run if there are two or more U4164A logic analyzer cards in adjacent slots in a chassis.

This test verifies whether or not the flex cables are squarely and firmly inserted into the connectors.

Comparator Programming Test

The purpose of this test is to verify the programming path to each of the comparators.

Comparator/DAC Test

This test is executed only if all probes are detached.

This test uses the pod, bonus, and calibration DACs, the calibration oscillator (implemented in the interface FPGA), the comparators, the connections between the comparators and the Analysis chip, and the activity indicators in the Analysis chip. We verify that we can use the DACs to control the data input to the comparators. We verify that each comparator data channel produces output. We verify that each comparator output is connected to each ASIC data input.

Comparator Delay Test

The comparator delay test verifies the integrity of all the delay line elements for each delay line in the comparators. Each delay line consists of 11 delay elements. When set for maximum delay, all 11 elements are connected in series. If any element is faulty, then data will not propagate through the comparator. If this is the only test failing, then it is almost certainly a bad comparator.

Comparator Zero-Hold Cal Test

Tests the delay elements for each delay line in the comparators. It tests that each delay line can increase its delay in a linear way through a range of delay values.

Comparator Calibrations Test

The purpose of this test is to verify that each of the comparator one-time calibrations can successfully be performed. This verifies that all of the calibration circuitry and components are within the tolerance limits required for proper calibration. This test is executed only if all probes are detached.

Acquisition Memory Write/Read Test

This test checks that each acquisition chip can write data to DDR acquisition memory and read the same data back.

Acquisition Memory Cell Test

Tests every bit of the DDR acquisition memory. The test verifies that every bit can be written to 0 and written to 1 and read back accurately.

ATB (AXIe Trigger Bus) Test

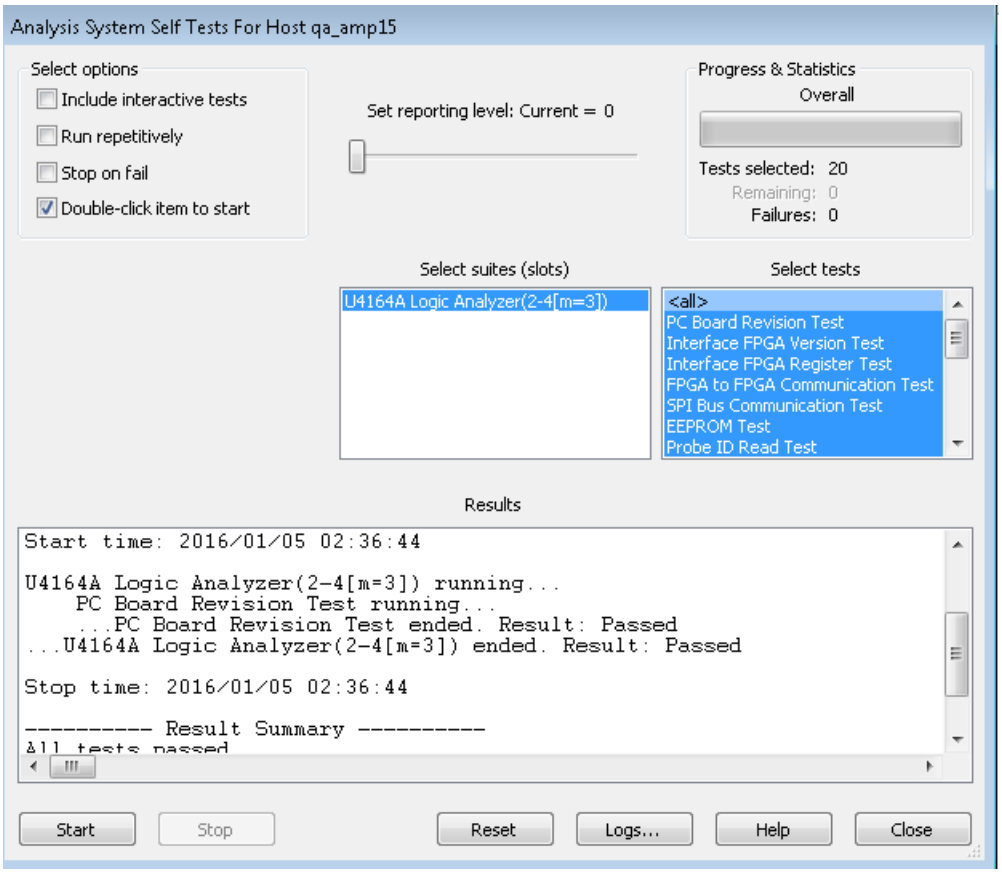
This test verifies the ATB signal connections between the acquisition chips, the interface FPGA and the two 8-bit transceiver chips.

To run the self tests

You can run self tests on the U4164A module to verify if the module is operating correctly. Before running self tests, ensure that:

- you have connected all the hardware components for the U4164A module
- created a logical module for U4164A in the Keysight Logic Analyzer application.
- disconnected all probes from the logic analyzer module.

You use the **Analysis System Self Tests** window to run self tests. Refer to the topic "Perform the Self-Tests" on page 21 to know how to run these tests.



If all tests did not pass, refer to "To use the flowcharts" on page 54.

To exit the test system

Close the self-test window. No additional actions are required.

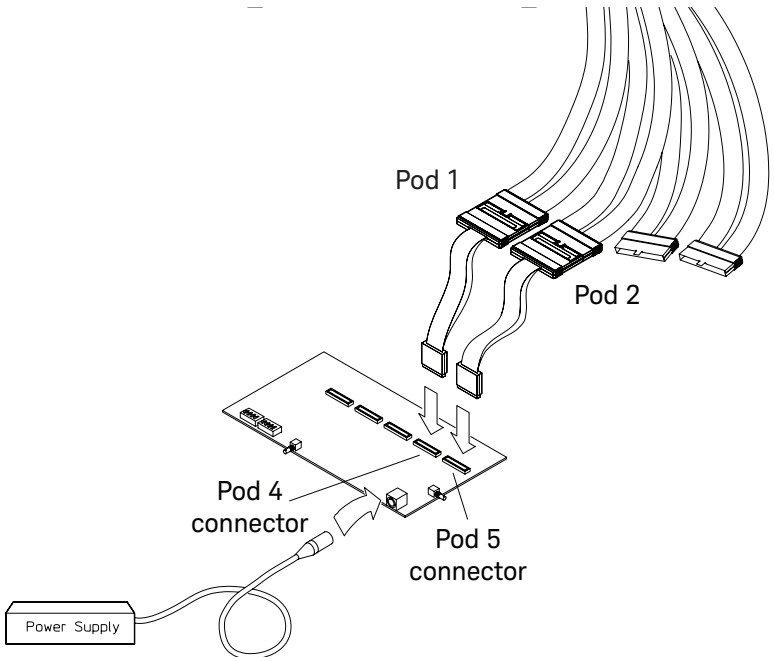
To test the cables

This test allows you to functionally verify U4201A logic analyzer cables and Keysight E5379A probes.

Table 4 Equipment Required to Test Cables

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001
Differential Probes	No Substitute	E5379A (Qty 2)

1 Connect the U4164A logic analyzer to the stimulus board.
   a Connect the Keysight E5379A 90-pin differential probes to the logic analyzer cable (also called "Pods") to be tested. Start with Pods 1 and 2.
   b Connect the E5379A probe from logic analyzer Pod 1 to connector "Pod 4" on the stimulus board.
   c Connect the E5379A probe from logic analyzer Pod 2 to connector "Pod 5" on the stimulus board.
   d Connect the stimulus board power supply output to the stimulus board power supply connector J82.
   e Plug in the stimulus power supply to line power. The green LED DS1 should illuminate showing that the stimulus board is active.



2 Set up the stimulus board

a Configure the oscillator select switch S1 according to the following settings:

- S1 0 (Off).
- S2 1 (On).
- S3 0 (Off).
- Int.

b Configure the data mode switch S4 according to the following settings:

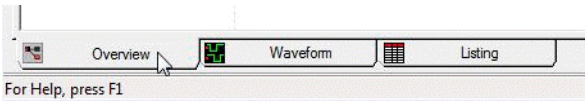
- Even.
- Count.

c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

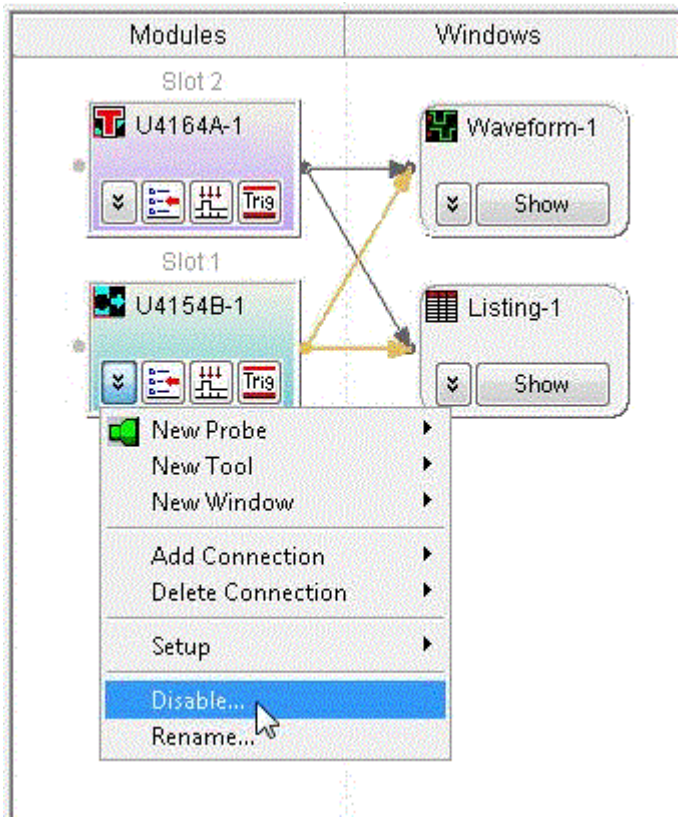
3 In the *Keysight Logic and Protocol Analyzer* application, choose **File→New**. This puts the logic analysis system into its initial state.

4 Disable all analyzers except the one being tested. This simplifies the instructions and makes module initialization faster.

a Select the **Overview** tab at the bottom of the main window.

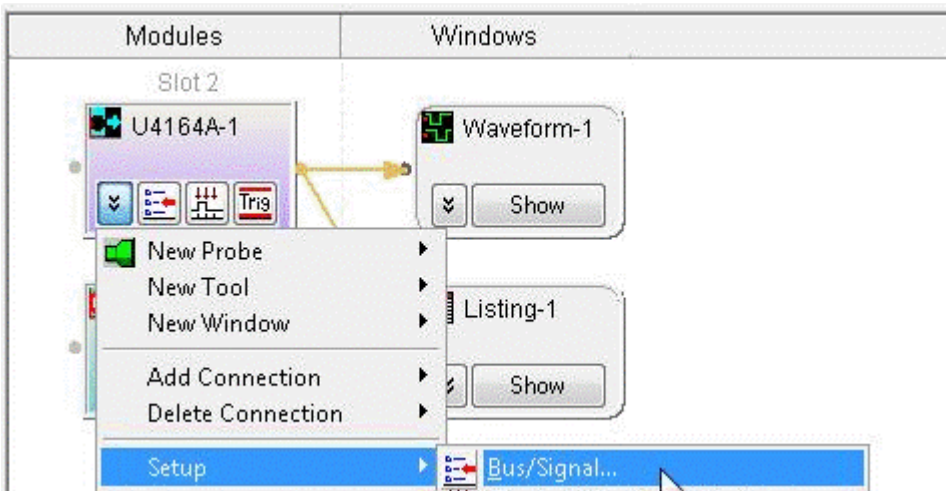


b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.

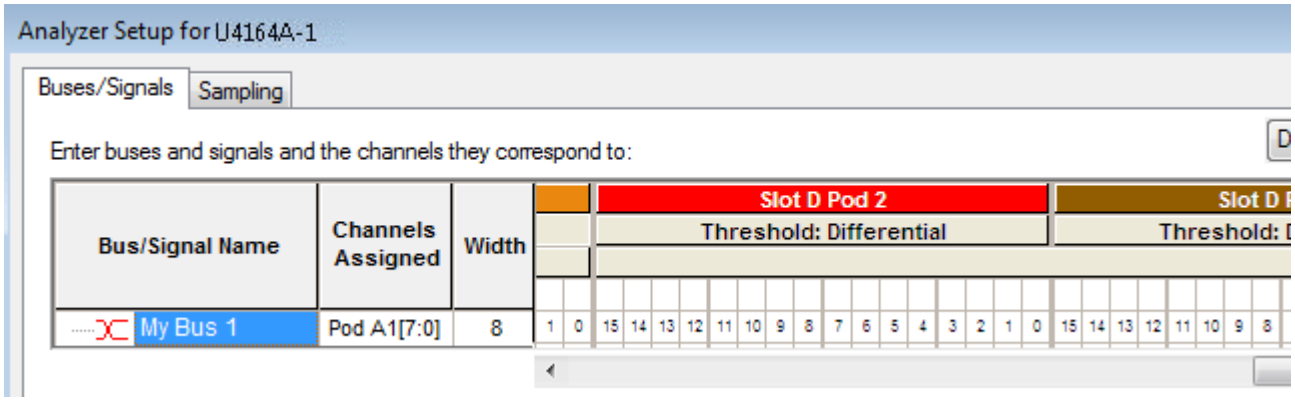


5 Set up the bus:

a In the **Overview** window, select **Setup -> Bus/Signal...** from the module's drop-down menu.

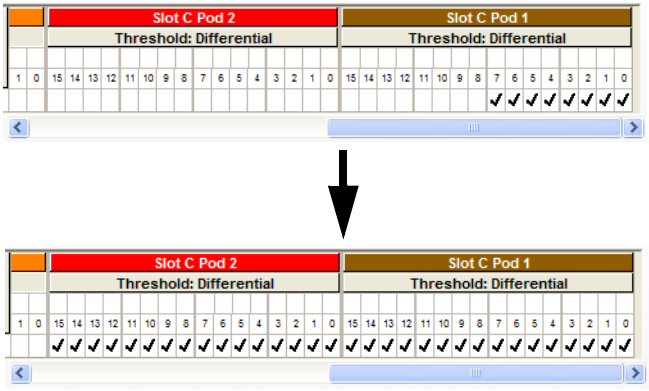


b Scroll if necessary to view the pods you are testing.



c Verify that the pod threshold buttons say "**Threshold: Differential**", as shown above. If they don't, make sure the correct probes (E5379A) are attached to pods 1 and 2. The threshold is set to Differential automatically when E5379A probes are attached.

d Channels 7 through 0 are already assigned by default. Assign pod 2 channels 15 through 0 and pod 1 channels 15 through 8 by clicking and dragging from the left-most channel box to the right-most channel box. Your display should look like the lower picture when you are done.

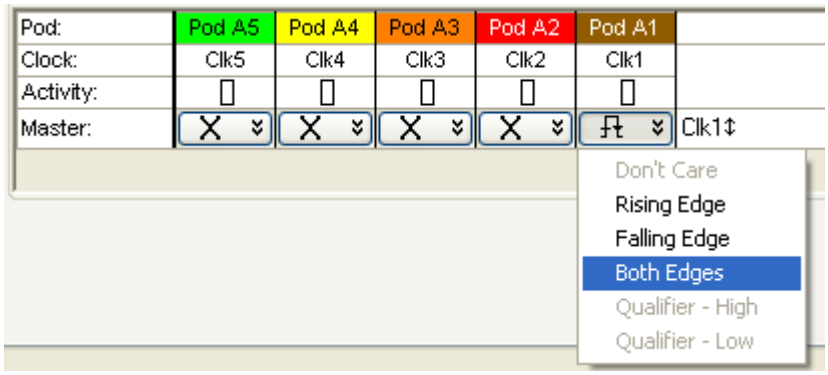


6 Select the State sampling mode and set the State Clock options:

a Select the **Sampling** tab of the Analyzer Setup window.

b Select **State - Synchronous Sampling**.

c For State Clock, select **Pod A1 Clock** and **Both edges**.



7 Set the trigger position and acquisition memory depth:

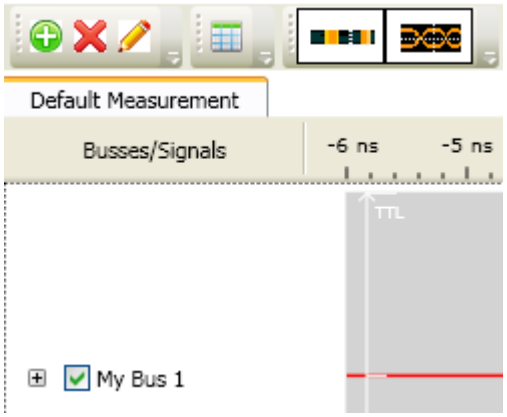
a Set the Trigger Position to **100% Poststore**.

b Set the **Acquisition Depth** to **8K**.

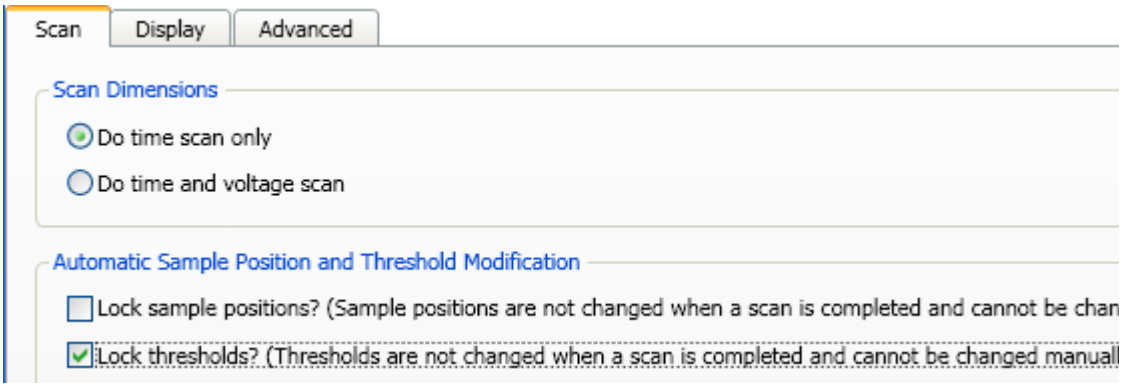
8 Adjust sampling positions:

a Select the **Eye Scan: Thresholds and Sample Positions** button. The Eyescan - Sample Positions dialog will appear.

b In the “Busses/Signals” section of the Eyescan - Sample Positions dialog, make sure the check box next to “My Bus 1” is checked.



c Click **Edit** and select the **Do time scan only** option as the scan dimension and the **Lock Thresholds** checkbox.



d Select the **Run This Measurement** button in the **Eyescan - Sample Positions** dialog.

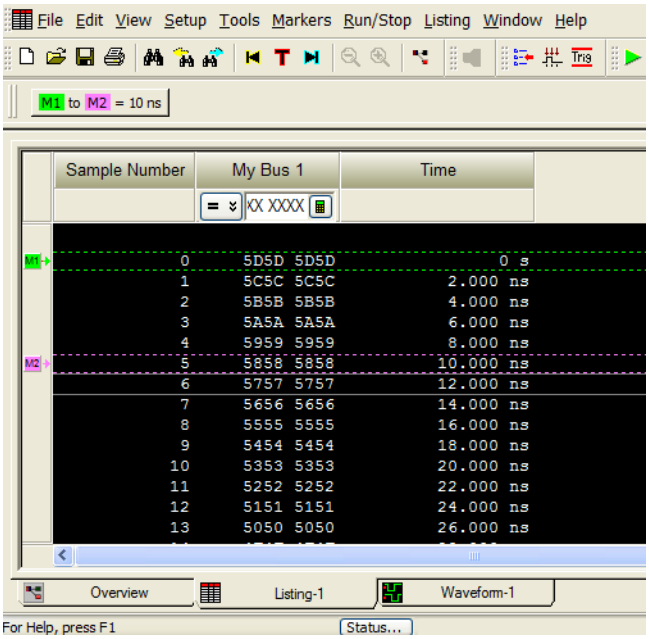
e Make sure the sampling positions are set properly, and re-align any stray channels if necessary.

f Select **OK** to close the **Eyescan - Sample Positions** window.

g Select **OK** to close the **Analyzer Setup** window.

9 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

10 Select the Run icon  . The listing should look similar to the figure below when you scroll down a bit.



Scroll down at least 256 samples to verify the data. **My Bus 1** shows four 8-bit binary counters decrementing by 1. If the listing does not look similar to the figure, there is a possible problem with the cable or probe. Cause for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

If the test data is not correct, then perform the following step to isolate the failure.

11 Verify the failure:

a Swap the E5379A probes so that the pod 1 cable remains connected to the stimulus board's pod 4 connector and the pod 2 cable remains connected to the stimulus board's pod 5 connector – just using different probes.

b Select the **Run** icon  .

If the failure is the same (that is, the error follows the cable) then the cable is faulty.

If the failure switches pods (that is, the error follows the E5379A probe) the probe is faulty.

12 Repeat the cable test for pods 3 and 4:

a Connect the logic analyzer's pod 3 cable to the stimulus board's pod 4 connector.

b Connect the logic analyzer's pod 4 cable to the stimulus board's pod 5 connector.

c In the **Busses/Signals** tab of the Analyzer Setup window, assign the pod 3 and 4 channels to "My Bus 1".

d In the **Sampling** tab of the Analyzer Setup window, for State Clock, select **Both edges**.

e Adjust sampling positions.

f Select the **Run** icon  . In the Listing window, check at least 256 samples for failures; if necessary, verify any failures by swapping the E5379A probes.

13 Repeat the cable test (step12) for pod pairs 5 and 6 and 7 and 8 connecting the odd pod cable to the stimulus board's pod 4 connector and the even pod cable to the stimulus board's pod 5 connector:

14 Return to the troubleshooting flowchart.

6 Returning and Replacing a U4164A Module or its cables

To remove the U4164A module / 68
To remove the logic analyzer cable / 68
To install the logic analyzer cable / 68
To replace the circuit board / 69
To return the U4164A module or cable for Repair/Exchange / 70

This chapter contains the instructions for removing and replacing the U4164A logic analyzer module, and the probe cables of the module as well as the instructions for returning defective parts to Keysight Technologies.

CAUTION

Turn off the AXIe chassis before installing, removing, or replacing a module in the chassis.

The enclosure surface of the U4164A module may become hot during use. If you need to remove the module, first power down the AXIe chassis, allow the module to cool, and then pull the module out of the chassis.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

To remove the U4164A module

If the U4164A module or any of its parts are faulty, remove the faulty module from the AXIe chassis, return it to Keysight Technologies for repair/exchange. On getting a replaced module, install it in the AXIe chassis.

Instructions for removing or installing the module into the AXIe chassis can be found in the *AXIe based Logic Analysis & Protocol Test Modules Installation Guide*.

To remove the logic analyzer cable

If you are using a probe/interposer that requires a logic analyzer cable such as a U4201A cable or a U4208A cable, then the following procedure is applicable .

There are four cables for each U4164A logic analyzer module. One cable is for pods 1 and 2, the other cable is for pods 3 and 4, and so on till pod 8 of the U4164A module. The following figure displays three cables attached to pods 3, 4, 5, 6, 7, and 8 of the U4164A module.

To remove the logic analyzer cable:

1 Remove power from the AXIe chassis
   a Turn off the chassis.
   b Disconnect the power cord.
2 Remove the logic analyzer pod cable.
   a Remove the two thumb screws that secure the logic analyzer cable to the pods in the front panel of the module.
   b Disengage thumb screws completely from the module.
3 Pull the cable straight out from the front panel of the module.

If the logic analyzer cable is faulty, return it to Keysight Technologies for repair/exchange or order a new cable which is available as a replaceable part, and follow the next procedure to install the replaced logic analyzer cable.

To install the logic analyzer cable

Perform the following steps to connect the new/replaced logic analyzer cable to the front panel of the U4164A module.

1 Attach cable connector to the pod input on the front panel of the module.
2 Tighten the two thumb screws on both sides of the cable to retain the cable tightly inside the relevant pod input. Do not over tighten the thumb screws. Hand tightening is recommended or maximum torque of 3in-lb.

To replace the circuit board

If the circuit board of the U4164A module is found faulty, perform the following steps to get it repaired/replaced.

1 Remove the logic analyzer cables using the “To remove the logic analyzer cable” procedure on page 68.

2 Remove the U4164A module with the faulty circuit board from the AXIe chassis. Refer to the *AXIe based Logic Analysis & Protocol Test Modules Installation Guide* to learn how to remove the module from chassis.

3 Send the U4164A module to Keysight Technologies to repair or replace the faulty circuit board with a new circuit board.

To return the U4164A module or cable for Repair/Exchange

Before returning the U4164A module or a logic analyzer cable to Keysight Technologies, contact your nearest Keysight Technologies Sales Office for additional details. Information on contacting Keysight can be found at www.keysight.com.

1 Write the following information on a tag and attach it to the module/cable.
   - Name and address of owner.
   - Model number.
   - Serial number.
   - Description of service required or failure indications.

2 Remove accessories from the module.

   Only return accessories to Keysight Technologies if they are associated with the failure symptoms.

3 Package the module/cable.

   You can use either the original shipping containers, or order materials from an Keysight Technologies sales office.

CAUTION **For protection against electrostatic discharge (ESD), package the module in ESD-safe material.**

4 Seal the shipping container securely, and mark it FRAGILE.

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